Growth and Interface Engineering of Highly Strained Low Bandgap Group IV Semiconductors

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1. Introduction

To further improve the performance and power consumption of integrated circuits (IC) alternative channel materials to Silicon (Si) as well as novel device concepts attract more and more research interest. Especially, Germanium (Ge) is a promising candidate for several reasons. First, Ge offers the highest bulk hole mobility of any known semiconductor material [1] promising high p-MOSFET performances in terms of drive currents. On the other hand, due to its low and quasi-direct bandgap, Ge is also used for low power devices such as Tunnel-FETs [2]. These properties might be even enhanced by strain engineering or alloying Ge with Sn [3,4]. However, introducing high biaxial tensile strain in Ge or GeSn remains a challenge because of missing adequate buffer technology. High quality CVD epitaxy of GeSn layers enables a new degree of freedom in Ge(Sn) strain engineering.

In this contribution, we will present the epitaxial growth of highly tensely strained Ge and GeSn layers up to 1.4 % and 0.4 %, respectively, using high Sn-content (Si)GeSn buffer layers. In this context, electronic band structure calculations including effective masses at certain points in the Brillouin zone will be provided. In Fig. 1 the bandgap narrowing induced by strain is highlighted. Applying 1.4 % tensile strain results in a bandgap reduction of 162 meV and an energy difference between \( \Gamma \)- and L-valley of solely 14 meV. Via MOS-capacitors (MOSCAPs) the surface passivation as well as interface quality of the low bandgap materials is addressed. In this context, the CMOS process limitations towards integration concerning strain preservation and Sn segregation are discussed.

2. Experimental

(Si)GeSn buffer layers on Ge virtual substrates (GeVS) were epitaxially grown by Reduced-Pressure CVD (RP-CVD). Ge(Sn) layers grown on high Sn

3. Results and Discussion

In order to tensely strain Ge we employ lattice engineered GeSn buffers with large in-plane lattice constants. Here, high Sn content can be achieved due to low growth temperatures 350°C and high growth
rates at the same time. In Fig. 2a a TEM micrograph of 250 nm Ge$_{0.86}$Sn$_{0.14}$ is shown. This layer thickness exceeds the critical thickness for strain relaxation by far resulting in plastic strain relaxation. Hence, a high density of misfit dislocations was observed at the GeSn/Ge-VS interface but no dislocations, e.g. threading dislocations, were found in the top part of the layer. With this technique strained Ge layers with thicknesses up to 70 nm and maximum strain of 1.4% were fabricated.

Exemplary, XRD-RSM data of a strained Ge/GeSn/Ge-VS structure are presented in Fig. 2b. Here, a Ge$_{0.91}$Sn$_{0.09}$ buffer layer with a degree of strain relaxation of 61 % was employed and a strain level of about 1 % was measured in the Ge top layer. A crucial step towards device integration of these highly strained materials is the gate stack formation.

4. Conclusions

Highly tensile strained Ge(Sn) layers epitaxially grown on GeSn strain relaxed buffer layer have been presented. Electrical characterization exhibits good interfacial quality of the high-k gate stacks employing HfO$_2$ on Ge and strained Ge. These results mark a first step towards electronic device integration of low bandgap highly tensely strained group IV semiconductors.

References