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Citation: Journal of Applied Physics **86**, 6924 (1999); doi: 10.1063/1.371774
View online: http://dx.doi.org/10.1063/1.371774
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/86/12?ver=pdfcov
Published by the AIP Publishing

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(Received 14 June 1999; accepted for publication 13 September 1999)

We report a study of metal–insulator–semiconductor (MIS) structures on InP. The interfacial state density and deep levels existing in MIS structures were measured by deep level transient spectroscopy (DLTS) technique. The electrical insulator properties were measured by current–voltage techniques. MIS structures were fabricated on InP substrates by direct deposition of silicon nitride (SiN$_x$:H) thin films by electron cyclotron resonance chemical vapor deposition. In this work, we show that interfacial state density can be diminished, without degrading electrical insulator properties, by fabricating MIS structures based on a dual layer insulator with different compositions and with different thickness. The effect of rapid thermal annealing treatment has been analyzed in detail in these samples. Interface state densities as low as $3\times10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ were measured by DLTS in some structures. Conductance transients caused by disorder-induced gap states have been observed and analyzed providing some information about interface width. Finally, deep levels induced in the substrate have been investigated. Three deep levels at energies of 0.19, 0.24, and 0.45 eV measured from the conduction band have been found, and their dependence on the rapid thermal annealing process has been analyzed. © *1999 American Institute of Physics.* [S0021-8979(99)03824-4]

I. INTRODUCTION

Great interest has been concentrated on InP metal–insulator–semiconductor (MIS) devices due to their promising advantages for high-frequency field-effect transistors (MISFET), because of the fact that indium phosphide has a high mobility and a low surface recombination velocity.[1] However, some problems related to interfacial traps still remain in InP MIS devices. In particular, interfacial traps are responsible for current drift in InP MISFETs,[2–4] cause undesirable leakage currents, shifts in threshold voltage, and reductions in the transconductance of MISFETs. The interface between native oxide and InP presents a high interfacial state density, therefore, it has been necessary to try different insulators to fabricate MIS structures on InP with improved interfacial properties. The SiO$_x$/InP[5,6] and the SiN$_x$/InP[7,8] are the principal structures insulator-InP developed. Silicon nitride layers have been extensively used as gate dielectrics in thin film transistors (TFTs),[9,10] as interlayer dielectrics, and as final passivation layers in integrated circuits. SiN$_x$ films are typically fabricated either by plasma enhanced chemical vapor deposition (PECVD) or low-pressure chemical vapor deposition (LPCVD) methods. In this work, the electron cyclotron resonance (ECR) plasma method[11] has been used. Due to the low ion energies (<25 eV) in the ECR plasma,[12] and the low processing temperature, this deposition technique provides ''soft'' deposition conditions that minimize the semiconductor surface degradation during the insulator deposition. Nitride films were deposited as a function of the gas flow ratio, $R=[\mathrm{N_2}]/[\mathrm{SiH_4}]$, which was modified to vary the insulator stoichiometry, that is, the nitrogen content, x, in the SiN$_x$ layers.

The aim of this work is to fabricate a new indium phosphide MIS structure using a dual layer (SiN$_x$:H) insulator, and characterize its electrical properties. Four electrical characterizations have been employed: first, interfacial state density has been measured by deep level transient spectroscopy (DLTS); second, conductance transient measurements and $C-V$ technique were used. Then electrical insulator properties (resistivity and electrical breakdown field) have been obtained by $I-V$ measures. And, finally, we have characterized deep levels existing in the InP substrate by DLTS.

II. SAMPLE DESCRIPTION

A. Preliminary studies

In previous works,[13,14] we have studied the influence of the nitrogen content in the interface quality, and insulator film properties of dielectric layers deposited on different substrates. In particular, the samples studied were Al/SiN$_x$:H/Si and Al/SiN$_x$:H/InP. Opposite trends were obtained for the two substrate semiconductors. In the present work, we focus

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our attention on the $Al/SiN_x:H/InP$ MIS devices study. The insulator composition and the density of interface traps are inversely correlated. The minimum interfacial trap density concentration was obtained for the films with the maximum [N]/[Si] ratio, $R=9$, corresponding to $x=1.55$, that is, highest nitrogen content in the insulator. The decrease of interfacial defects as the insulator stoichiometry changes is explained in terms of a substitutional mechanism: N atoms coming from the insulator may be located at phosphorus vacancies, V_P, giving rise to N_{V_p} configurations.[14]

However, the dielectric behavior of the insulator-resistivity, ρ, and electrical breakdown field, E_{B^-}, is not the best for this concentration value ($x=1.55$), because of the low values of resistivity, and the low electrical breakdown field. Nevertheless, when the nitrogen content decreases ($x=1.43$), the resistivity and electrical breakdown field become higher. Besides, the dielectric constant tends to be higher in silicon-rich films, and lower in the films with excess nitrogen.[15] In conclusion, although a high nitrogen content insulator favors low interfacial state density, the electrical properties are simultaneously degraded. A reverse behavior is detected for low nitrogen content insulator layers where the electrical properties improved, whereas the interfacial trap density increased.

As a result of this previous work, we have developed our samples improving both electrical insulator properties, and insulator state density, avoiding the utilization of usual passivation procedures of the InP surface prior to the insulator deposition. To reach this, several approaches were developed:

(a) The use of a dual-layer gate insulator structure which combines different stoichiometry layers to optimize both interfacial and electrical insulator properties. This strategy is widely used in Si-based technology (Lucowsky ONO structures),[16,17] but is scarcely used in III–V semiconductor technology.

(b) Rapid thermal annealing (RTA) treatment at temperatures between 400 and 800 °C during 30 s which improves the interfacial state density.

(c) Optimization of the gate insulator thickness to minimize the stress[18] and reduce the interfacial state density.

B. Fabrication of samples

Substrates were undoped (100) *n*-type InP fabricated by liquid encapsulated Czochralski (LEC), with an unintentional dopant concentration of $5\times10^{15}\,cm^{-3}$. The MIS structures were fabricated by directly depositing silicon nitride films on InP wafers with the ECR plasma method. The deposition temperature was 200 °C.

The devices were fabricated as follows: previous to the insulator deposition, wafers were cleaned with organic solvents, etched during 1 min in a $HIO_3:H_2O$ (10% at weigh) and immersed in $HF:H_2O(1:10)$ soak for 15 s to strip the native oxides. Finally, samples were rinsed in deionized water and dried in N_2. Subsequently, sets of six samples were transferred to the insulator deposition chamber. The deposition was carried out according to the following parameters: the substrates were heated at 200 °C and a total pressure of 0.6 mTorr was kept constant during the deposition process. Microwave power was also kept constant at 100 W. The gases used were N_2 and pure SiH_4. The gas flux ratio, $R=[N_2]/[SiH_4]$, ranged from 1.6($x=1.43$) to 9($x=1.55$).

For the dual-layer insulator samples, the insulator deposition was performed in two steps in which the gasses flux was controlled to obtain the different stoichiometries. The two steps were carried out sequentially in the same deposition run, and under the same conditions of power, temperature and pressure described above. First, a layer obtained at $R=9$ ($x=1.55$) was directly deposited on the InP surface and was named ''bottom layer,'' and, then, an $R=5$ ($x=1.43$) layer was subsequently deposited (''top layer''). Two different insulator thicknesses were analyzed: type A samples with a total thickness of 500 Å, where the thickness of each layer is 100 Å for the bottom layer and 400 Å for the top one; and type B samples, with a total thickness of 200 Å (50 Å for the bottom layer and 150 Å for the top layer).

After deposition, the RTA process was carried out in Ar atmosphere. Argon is one of the most common inert gasses used for RTA, and its purity degree is higher than the obtained for N_2 gas, which occasionally can contain O_2 and oxidize the surface. The annealing temperature ranged between 400 and 800 °C, and the time was kept constant at 30 s (preliminary studies reveal that annealing effects are stable for times longer than 20 s). One sample of each type is kept unannealed to be used as a control one, and the other five samples of each type were annealed at 400, 500, 600, 700, and 800 °C.

A set of single-layer insulator samples was also fabricated for comparison. The insulator deposition was performed with the same conditions described above for 22 min, the time necessary to obtain an insulator thickness of 500 Å. This group of samples corresponds to an insulator stoichiometry of $x=1.55$ ($R=9$). These samples were used as controls, which were also annealed under the same RTA conditions described previously.

Afterwards, Al dots ($1.2\times10^{-3}\,cm^2$) were thermally evaporated with a mechanical mask. Finally, an AuGe/Au back electrode was evaporated. A post-metallization annealing was performed in Ar atmosphere (300 °C/20 min).

Finally, in order to be able to separate the effects of insulator ECR deposition from those of RTA processing or even from the potential native defects of the ''as-grown'' compound semiconductor, a ''virgin'' sample was also kept for comparison: a non insulator deposited, non-RTA treated *n*-type InP sample. A Schottky diode on this crystal was produced by evaporation of a gold film in an ultrahigh vacuum system.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Interfacial state density

In order to achieve the interfacial state density for the different MIS structures along with its dependence on the structure and stoichiometry of the insulator layer and on the RTA processing, DLTS measurements between 78 and 300 K were used to characterize the devices. The experimental setup consists of a 1 MHz Boonton 72B capacitance meter

and a HP54501A digital oscilloscope to record the complete capacitance transients. A Keithley 617 programmable electrometer and a HP214B pulse generator were used to introduce the quiescent bias and the filling pulses, respectively. The D_{it} distribution was deduced from DLTS measurements by means of the expressions;[19]

$$D_{it}=\frac{\epsilon_s}{KT}N_D\frac{C_I[C(t_2)-C(t_1)]}{[C(t_3)]^3}\frac{1}{\ln(t_2/t_1)}, \tag{1}$$

$$E=Ec-KT\ln\left[\sigma_n(E)v_{th}N_C\frac{t_2-t_1}{\ln(t_2/t_1)}\right], \tag{2}$$

where $C(t)$ is the capacitance evaluated at time t, C_I is the capacitance of the insulator, σ_n is the interface states capture cross section, v_{th} is the thermal velocity of electrons, and N_C is the effective density of states of the conduction band. An energy-independent capture cross section value of $\sigma_n=1\times10^{14}\,\mathrm{cm}^2$ was used in the calculation,[20] which is typically found in InP MIS structures.

When the states are distributed both in energy and space, DLTS measurements tend to underestimate[21,22] the D_{it} of states near E_c rather than the D_{it} of states near the midgap of which DLTS signal goes through the maximum at around room temperature.

Figure 1 shows the D_{it} distribution obtained from DLTS measurements for the devices with different insulator compositions described previously. The presence of a maximum located at about 0.19 eV below the edge of the conduction band is detected. Several measurements with different saturating pulses and with different bias voltage were carried out, and since the height and temperature position of the DLTS peak do not change with the pulse,[23,24] this trap is associated to a deep level. This deep level has been found in some of the samples of our study and further discussion will be considered later.

A large increase of DLTS signals at high temperatures is observed, as a consequence of the minority-carrier thermal generation.[24] At high temperatures the depletion to inversion relaxation time constant of MIS capacitors due to minority carrier generation falls into the DLTS time constant yielding an apparent emission peak.

In this part of our study, we focus our attention on the dependence of the interfacial state density on the insulator composition, and on the RTA temperature with a double purpose. First, to gain an insight into its physical nature and, second, to achieve the optimum technological conditions for device manufacturing.

In a previous work,[25] we studied the hydrogen content of the films and its evolution with RTA temperature. The RTA process gives place to a reorganization of Si–H and N–H bonds at the insulator films. The hydrogen content and its evolution with RTA is temperature dependent.

D_{it} have been plotted in Fig. 1 for the three series of samples, i.e., type A, type B, and controls. The dependence of D_{it} profiles on the RTA temperature follows the same trend for the three series of samples. As can be observed, D_{it} profiles decrease for samples annealed at temperatures of 400 and 500 °C, whereas the interfacial damage increases for the samples annealed at temperatures higher than 500 °C.

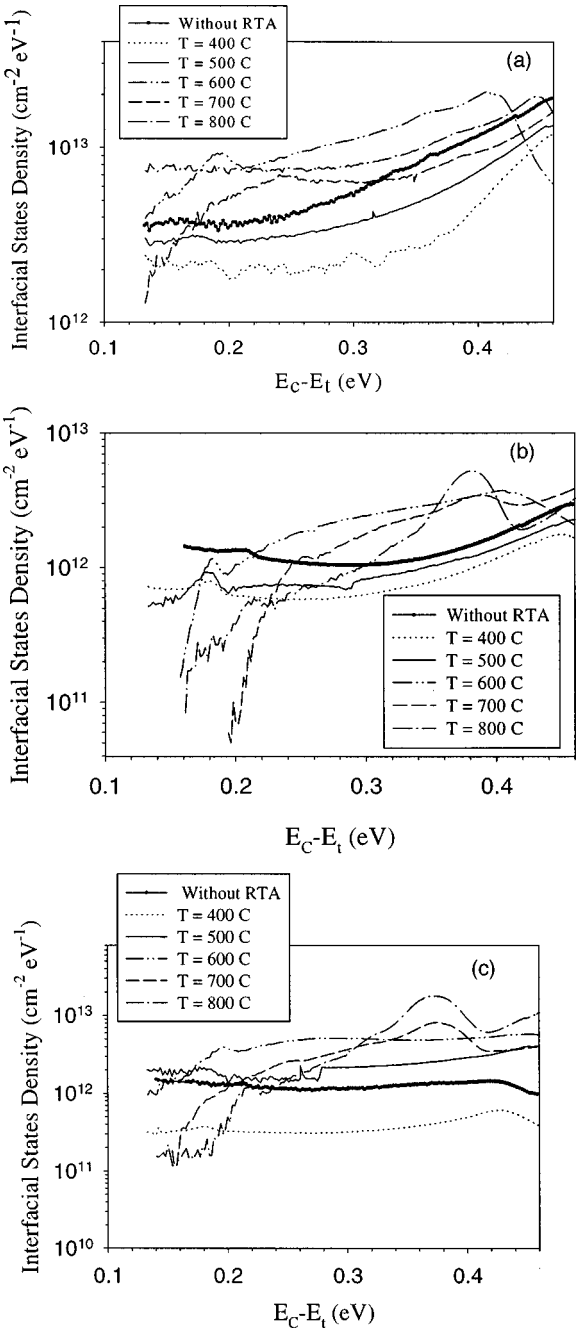

FIG. 1. Interfacial state density measured by DLTS technique for: (a) single-layer insulator (control) samples, (b) type A dual-layer insulator samples with 500 Å insulator total thickness, and (c) type B dual-layer insulator samples with 200 Å thickness total insulator.

A significant difference in the absolute interfacial state density value must be pointed out for each series of samples. For control single-layer samples, D_{it} is kept in the range of $1-8\times10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, Fig. 1(a). However, for the dual-layer samples, the interfacial state density becomes lower. In particular, for the type A samples (500 Å total insulator thickness), D_{it} remains in the range of $0.4-2\times10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, Fig. 1(b). Finally, for the type B dual-layer samples (200 Å total insulator thickness), the lowest interfacial trap density is obtained. For these samples, D_{it} appears in the range of $0.3-4\times10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, Fig. 1(c). Therefore, we can conclude that the interfacial state density

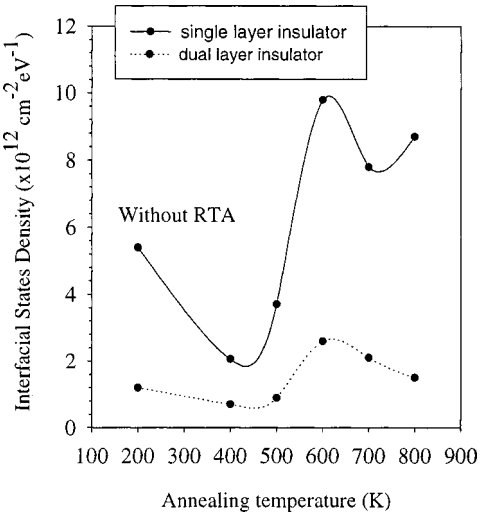

FIG. 2. Interfacial state density as a function of RTA temperature for the single layer, and for the type A dual-layer insulator sample with 500 Å insulator total thickness. D_{it} has been measured at a fixed energy from the conduction band. The ''unannealed'' sample is placed at 200 °C because this was the temperature at which the ECR process was carried out.

has been improved for both dual-layer structures and, in particular, the biggest improvement corresponds to the type B samples having the lowest insulator thickness.

In Fig. 2, the dependence of D_{it} on RTA temperature has been plotted for the type A (500 Å thickness) dual-layer insulator samples, and for the single-layer insulator (control) samples. As it is shown, thermal treatment induces a decrease in the interfacial state density when annealing temperature remains lower than 500 °C, but, beyond this temperature, D_{it} increases. Consequently, a D_{it} minimum is observed corresponding to samples which have undergone an RTA treatment at 500 °C. That can be tentatively explained as follows: the surface of InP becomes defective by the loss of the most volatile element (phosphorus) when this surface is chemically cleaned or plasma exposed. Even in the case of low temperature treatments[26] or remote plasma exposure, such as ECR, a loss of P has been reported.[13] Therefore, a defective surface is generated where phosphorus vacancies (V_P) are present, making the semiconductor unable to be used in electronic devices, e.g., FETs, where the surface quality is a critical issue. Nevertheless, since ECR is a remote plasma method, the induced amount of V_P should remain much lower than that obtained by direct plasma methods. When a low temperature RTA treatment is applied to the sample, some intermixing between the insulator and the semiconductor surface takes place.[13] In particular, nitrogen atoms of the insulator move toward the first atomic layers of the semiconductor surface. As a consequence, N atoms coming from the insulator may occupy phosphorus vacancies, V_P, giving place to N_{V_P} configurations. Thus, the interfacial state density decreases as the phosphorus vacancy density does, due to the V_P effective passivation produced by N atoms. On the other hand, when a high temperature RTA treatment is applied, the evolution is different. In previous works,[25,27] it has been proved that a loss of nitrogen takes place at annealing temperatures higher than 500 °C. Thus, the passivation by N atoms is diminished, increasing the V_P concentration, and, consequently, the interfacial traps density is increased again.

It may be suggested that RTA treatment gives rise to two simultaneous and opposing processes, whose balance is temperature dependent. For the lower annealing temperatures, below 500 °C, the V_P passivation effect is dominant, causing D_{it} to decrease. For annealing temperatures higher than 500 °C, the nitrogen loss from the phosphorus vacancies dominates, decreasing the above passivation and, as a result, D_{it} increases.

As for the dependence of transition temperature on dielectric stoichiometry we are now involved in a project in which MIS structures with different insulator compositions are being studied to analyze this dependence.

B. Disorder-induced gap state (DIGS)

We have experimentally observed that MIS C–V curves exhibit hysteresis phenomena. This behavior can be explained by the model proposed by He *et al.*[28,29] who suggested that the interface states are distributed both in energy and in space. In the spatial dimension, the regions of distorted local bonds extend on both sides of the interface, resulting in disordered regions both in the semiconductor and in the insulator. According to cross-sectional transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) studies,[30] the spatial extension of the disordered semiconductor region is very narrow, typically one or several monolayers, whereas that of the disordered insulator region reaches several tens of angstroms. The shape of the DIGS distribution is exponentially decaying away from the interface into the insulator.[20] In this way, the interface quality can be characterized by two parameters: the interfacial state density (D_{it}) and the ''width'' of the disordered insulator region. Both features are zero for ideal interfaces.

As no information on the interface width can be derived from DLTS measurements and in order to get a more complete electrical characterization of the disorder interface, we have carried out additional measurements which provide some information about the disordered insulator width. In a previous work,[31] we have proposed and described in detail the conductance transients method. Room temperature conductance transients are obtained when pulses that drive MIS structures from deep to weak inversion are applied. Subsequent, capture processes take place in which the empty DIGS states trap electrons coming from the conduction band. This capture kinetics is time consuming. States located near the interface capture electrons more rapidly than those located farther away in the insulator bulk according to a tunneling assisted process. The distance covered by the front of tunneling electrons, x_c, during a time t is[29,32]

$$x_c(t) = x_{on} \ln(\sigma_{on} v_{thn} n_s t),$$

where x_{on} is the tunneling decay length, σ_{on} is the electron capture cross section value for $x=0$, v_{thn} is the electron thermal velocity, and n_s is the free electron density at the interface. Following this expression, the front of tunneling

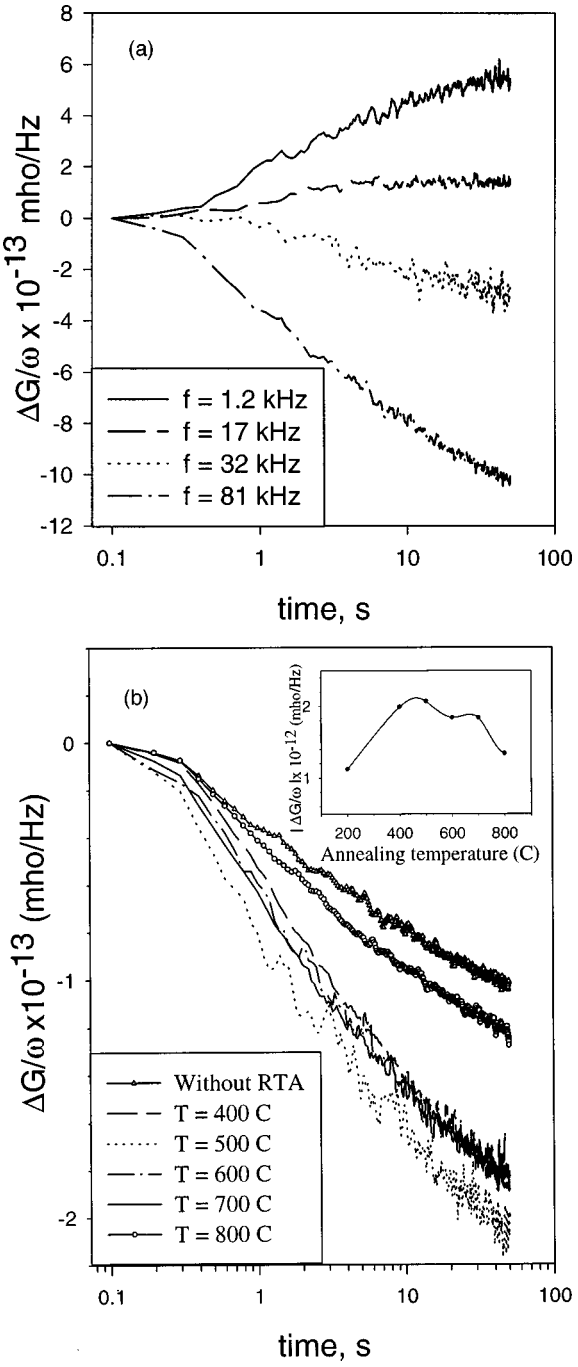

FIG. 3. Room temperature conductance transients for: (a) the single-layer insulator ''unannealed'' (control) sample at several frequencies, and (b) the single-layer insulator (control) samples at a fixed frequency of 81 kHz. The inset shows the maximum conductance transient amplitude ($\Delta G/\omega$), measured at a time of 50 s as a function of the RTA temperature.

electrons reaches depths of 183.7, 202.1, and 220.4 Å after times of 1, 10, and 100 s, respectively. Therefore, there is a direct relation between time and position of tunneling electrons into the insulator.

In Fig. 3(a), room temperature conductance transients at several frequencies are shown. Transients have been obtained by applying capture pulses to the single-layer insulator (control) sample without RTA treatment and recording the conductance signal. As can be observed, conductance transients are increasing for low frequencies whereas they are decreasing for high frequencies. This behavior agrees with the temporal evolution of the conductance measurement proposed in our previous work.[31] According to the explanation suggested in that work, only the decreasing transients provide reliable information about the interface states profile. Then, we focus our attention on transients measured at a frequency of 81 kHz.

In Fig. 3(b), decreasing transients at the frequency of 81 kHz are plotted for the single-layer insulator (control) samples set. As can be observed, the RTA treatment at different temperatures modifies the amplitude and the decay rate of the conductance transients. The inset on Fig. 3(b) shows the dependence of the conductance transients amplitude ($\Delta G/\omega$) on RTA temperature. Transient amplitude increases for samples annealed at temperatures of 400 and 500 °C, and becomes maximum at 500 °C. Nevertheless, for samples annealed at temperatures higher than 500 °C, the transient amplitude decreases. The same trend is observed for the transient decay rate. Thus, for samples annealed at temperatures of 400 and 500 °C, the decay rate increases, i.e., the transient is faster, reaching a maximum value for RTA temperature of 500 °C, and decreases for higher temperatures.

In summary, we have obtained identical evolution for D_{it} and the two above conductance transient characteristics on RTA temperature (Figs. 2 and 3, respectively). All of them reach critical points (maximum for the decay rate and $\Delta G/\omega$, and minimum for D_{it}) for an RTA temperature of 500 °C. In the case of D_{it}, the minimum value obtained at this annealing temperature means that the optimum interfacial state density and, then, the best interface quality are obtained at this temperature. Analogously, the maximum value of the conductance amplitude and the decay rate of conductance transients recorded at an RTA temperature of 500 °C might be related to the decay rate of the spatial distribution of the states profile into the insulator. As a conclusion, both the density of defects and the width of the interfacial region are optimized by carrying out the annealing treatment at a temperature of 500 °C.

C. Electrical insulator properties

The electrical insulator properties of the analyzed samples, resistivity, ρ, and electrical breakdown field, E_B, they are improved in the MIS structures based on the dual-layer insulator analyzed in this article. Electrical properties of the insulator films were obtained by measuring the $I-V$ characteristics of the MIS structures. The resistivity was calculated at an electric field of 1 MV/cm.[33] The value of E_B was determined as the field at which the MIS current, namely, the current across the insulator, reaches a value of 1 μA/cm^2.[34] The type A dual-layer sample exhibits the better values of the electrical properties, i.e., a resistivity of $2.6\times10^{14}\,\Omega$ cm, and a breakdown electric field of 1.7 MV/cm. Poorer values are obtained for the single-layer samples: $\rho=6\times10^{13}\,\Omega$ cm, and $E_B=1.2$ MV/cm, because their stoichiometry is the optimum in terms of interface state density, but is not the best for electrical breakdown and conductivity.

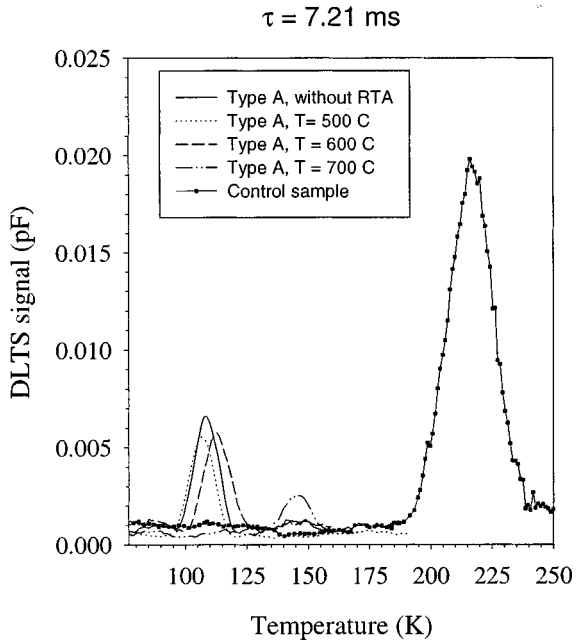

FIG. 4. Electron DLTS spectra for the InP virgin sample (without ECR deposition process and without RTA treatment), for the type A dual-layer MIS structures without RTA treatment, and for the type A dual-layer MIS structures with RTA treatment at several temperatures. DLTS spectra for MIS structures has been recorded only until 200 K because of the large increase in DLTS signal due to the thermally generated minority carriers arriving at the interface at higher temperatures.

D. Deep levels

We have determined and characterized the deep levels existing in the InP bulk by DLTS. Our study is focused on the MIS structures described above, where both deep levels and interfacial traps can be detected by DLTS measurements. According to Yamasaki *et al.*,[23] bulk traps can be distinguished from interface states experimentally. For interfacial traps, the shape and temperature position of the DLTS peak should change with the bias amplitude. On the contrary, in the case of the bulk traps with a discrete energy, the peak temperature should not change with pulse voltage, because the emission rate at a temperature is constant regardless of the pulse amplitude. In order to distinguish the interfacial traps from the bulk ones, several measurements with different filling voltage pulses were carried out. In this section, we summarize the peaks corresponding to deep levels located into the InP bulk.

First of all, in Fig. 4, we plot DLTS spectra for a control sample, that is, a Schottky diode with no insulator film deposition and no RTA treatment. An electron trap, labeled, E1 deep level has been found in this control sample whose corresponding emission energy is: $E_{E1}=E_C-0.45\,\mathrm{eV}$. According to this energy, this level could be related to phosphorus vacancies (V_P) or complexes involving V_P. Several studies [35–37] support this assignment.

DLTS spectra corresponding to type A samples have been also drawn in Fig. 4. As is shown in this figure, an electron trap, labeled as E2, is detected in samples which have solely undergone an ECR deposition process, and hence, no subsequent RTA treatment. Therefore, as an experimental conclusion, as this deep level does not appear in the control samples, the ECR process brings about this trap. The emission energy of the E2 center has been estimated as $E_C-0.19\,\mathrm{eV}$. This trap is detected in each annealed sample provided the annealing temperature is lower than 700 °C. However, for the annealed sample at a temperature of 700 °C, the E2 deep level disappears and a new peak, E3, whose emission energy is $E_C-0.24\,\mathrm{eV}$, is found. Thus, the E3 deep level can be classified as an RTA-induced center. Finally, if the sample is submitted to an RTA treatment at a temperature of 800 °C, the E3 trap vanishes. For the type B samples and the single-layer ones, the same deep levels and dependencies on the RTA process have been obtained.

Similarly to DLTS measurements for interfacial traps, DLTS measurements for deep levels in MIS structures are distorted at temperatures higher than 200 K due to the minority-carrier thermal generation that drives the MIS structure to the inversion regime. In consequence, we can not determine if the peak associated to the E1 trap does or does not appear for these samples.

Finally, in order to get an insight into the physical nature of the detected deep levels, we tentatively suggest some arguments which may play a role in the process. First of all, we have concluded that the E2 trap is an ECR-induced level. During the ECR process carried out for the deposition of the SiN_x:H dielectric layer, the InP substrate was kept at a constant temperature of 200 °C in a hydrogenated atmosphere. An unintentional hydrogenation of the substrate may occur as a consequence of this technological step. Hydrogenation of both GaAs and InP by H_2-plasma exposure can be found in the literature.[38,39] Moreover, the SiN_x:H layer has been reported[40] to be hydrogen permeable up to a width of approximately 200 Å. Therefore, atomic hydrogen may be able to penetrate InP substrate to some depth, to interact with defects in our case, V_P are excellent candidates[41–43] and/or impurities existing in this material, and even to participate in the generation of new defects.[39] In particular, complex defects involving one or several hydrogen atoms should not be ruled out.

For the annealed samples, no significant change is detected in the E2 level while the annealing temperature remains lower than 700 °C. In order to explain the complex behavior of the DLTS spectra at RTA temperatures of 700 °C and above, we might propose that an RTA-induced structural change occurs in the complex defect at 700 °C, giving rise to the E3 level and, eventually, this level is annealed out at 800 °C. The inherent instability of complex defects supports this hypothesis.

IV. CONCLUSIONS

In this work, we have developed a new MIS structure based on a dual-layer SiN_x:H insulator structure deposited on InP wafers by an ECR enhanced plasma method. These MIS devices are based on dual-layer insulator structures that combine two layers of SiN_x:H with different stoichiometries and optimize both interfacial state density and electrical properties of the insulator. An interfacial state density as low as $3\times10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$ has been achieved with these dual-

layer insulator structures. On the other hand, electrical properties of the dual-layer insulator have reached optimum values of $\rho = 2.6 \times 10^{14}\,\Omega$ cm, and $E_B = 1.7$ MV/cm.

RTA treatments at different temperatures have been applied to these samples. From DLTS and conductance transient measurements, we have concluded that the optimum interfacial state density value is obtained at an RTA temperature of 500 °C. This behavior can be tentatively explained by assuming that interfacial states are related to phosphorus vacancies at the wafer surface. RTA treatment passivates these defects by means of nitrogen atoms, giving place to V_{N_P} configurations. However, if RTA temperature increases over 500 °C, there are nitrogen losses[25,27] and the passivation diminishes so that the interfacial state density increases again.

We have also investigated the deep levels existing in the semiconductor bulk. For a ''virgin'' InP substrate: a native defect E1, located at $E_c - 0.45$ eV has been found which could be related to phosphorus vacancies. We have experimentally proved that the ECR process induces a new deep level, E2, located at $E_c - 0.19$ eV, which may be related to the fact that the substrate is exposed to a hydrogen-rich atmosphere. Finally, the RTA thermal process gives place to a final trap, E3, located at $E_c - 0.24$ eV, which anneals out at 800 °C.

ACKNOWLEDGMENTS

The authors would like to thank C.A.I. de Implantación Iónica from the Complutense University in Madrid for technical assistance with the ECR-CVD system. This work has been supported by the local Government Grant No. VA35/96 and by the Spanish government under Grant No. TIC 98/0740.

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