# A Portable Low-Cost SEU Evaluation Board for SRAMs

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*Abstract*— **This paper describes a field test system to evaluate the sensitivity of SRAMs to the natural radiation coming from the interaction of cosmic rays with the atmosphere. Unlike other experiments, this system is optimized to be portable and autonomous in order to allow making the development of the tests more flexible.**

*Index Terms*— **cosmic rays, neutrons, single event effects, SRAMs, soft error rate.**

## I. Introduction

ONE of the main challenges that the new generations of integrated devices must face is the increasing incidence of single event effects (SEE). These phenomena result from the impact of energetic particles (protons and heavy ions in the outer space, neutron or others at the sea level), issued from the interaction of cosmic-rays with the atmosphere, on the silicon lattice [1]. Indeed, a particle striking an integrated circuit may yield either the modification of the information stored in a memory cell (bit-flip or single event upset, SEU) or even the physical destruction of the device because of a thermal shock (e.g., single event latch-up, SEL) [2]. So far, these phenomena have been mainly observed in aircraft electronics [3], [4] (the neutron flux is 100-200 times higher at 10 km than that at sea level) but also in systems like the megacomputers [5] or systems largely distributed along the world (e. g., cardioverter defibrillators [6]). Moreover, in spite of some improvements that have brought a lower probability of single events (e. g., the absence of BPSG layer in new generation devices), the decrease of the transistor's features will lead to a likely growth of the figure of expected single events [7].

In this context, radiation tests are becoming compulsory in order to evaluate the radiation sensitivity of the commercial electronic devices. These tests are divided into two categories: *Accelerated radiation ground tests* and *field tests*. The former kind consists in exposing the *device under test, (DUT),* to a particle beam issued from a radiation facility such as a particle accelerator. This way, significant results can be obtained in a few hours although there is an important drawback: The access to the facilities is not easy due to the few number of them existing in the world.

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Another choice is to perform a so-called *field test*. In this case, no radiation facility is necessary since the devices are exposed to the natural radiation environment. Unlike advantages are evident, such as the possibility of developing the system to work anywhere, the drawbacks are also important. Indeed, natural radiation is not intense so the chance of observing single event effects is negligible unless the platform gathers a huge number of DUTs. Therefore, field test equipments are usually too voluminous so they are restricted to some research laboratories [8].

## II. Using SRAMs to Investigate the Sensitivity of a Specific Technology

Single event upsets are more likely to occur in devices including embedded SRAM cells [9]. Thus, devices such as SRAMs, microprocessors with integrated cache memory, FPGAs, etc. are liable to undergo a single event upset. Testing SRAMs is not a difficult task since it just consists in writing a preset pattern and cyclically verifying if the information has changed. On the contrary, microprocessors and FPGAs are hard to test, particularly due to the intrinsic difficulties to access to the sensitive area (i. e., configuration memory of an FPGA). For instance, in microprocessors, single event effects may lead to eventual crashes in the loaded program and no information about the kind and the place of the event can be obtained. On the contrary, events happening in unused memory cells do not affect the program behavior and they are never detected.

Nevertheless, the sensitivity to the environmental radiation does not differ much between SRAMS and other devices built in the same technology [10]. Therefore, field tests are usually performed on SRAMs, which are very easy to test, the results being extrapolable to other similar devices.

## III. Guidelines to design a portable system

As it was previously stated, a problem related to field test systems is their significant volume, which makes them difficult to transport by an only individual, mandatory condition in this experience, which requires to be installed in many different locations. Field tests' results speed up if the experiments are performed in high altitude facilities, such as the Mauna Loa [11] or the French Bures' Peak [12].

Hence, the advantages of a portable test evaluation board become evident. If such a system is developed, it can be carried anywhere to study the behavior of the devices, especially in promising places where the use of larger test systems are not suitable. In any case, this system must accomplish the following requirements:

1) Power autonomy
2) Wide temperature range
3) Ease to use and flexibility
4) Adaptability
5) Reliability
6) Radiation tolerance

In the following subsections, these points are discussed in detail.

### *A. Power Autonomy*

All of the portable systems are supposed to work in situations where the availability of external power supplies is not always guaranteed. This fact introduces significant constraints to the designer since not only must the system be autonomous but also optimized for a power consumption as lower as possible, due to the long duration of the tests. In the developed prototype, the first goal is achieved by means of the presence of a main power supply input, to be connected to an external source, and a secondary power input to attach a 7.2-V Ni-Cd battery. In some situations, the external source is replaced by a battery to make the system completely independent.

The power supply requirements also bring some problems to the design. Usually, computers, microprocessors or FPGAs are the instruments used to read the data stored in the DUTs. Nevertheless, these devices are characterized by a large power consumption that advises against their use. Thus, we decided to focus on CPLDs, from the FPGA's family but usually offering a very low power consumption in static mode (some tens of $\mu$A in the Xilinx' CoolRunner II family). The drawback of these devices is that they are not very large (32-512 cells) so the control system must be divided into independent blocks to fit in the devices.

A similar constraint affected the rest of devices. Therefore, all the components were selected among the low power families. Besides, usual clock generators based on quartz crystals were discarded since some custom relaxation oscillators have lesser power requirements. Hence, theses networks were used instead.

### *B. Wide temperature range*

Sometimes, the system must work in situations where the temperature can reach really low values, as it can be expected at the summit of a mountain or stratospheric balloons. Therefore, the use of industrial or military versions of the integrated devices is mandatory on the test board.

### *C. Ease to use and flexibility*

One of the purposes of the development of the evaluation board is to provide samples to volunteers inhabiting somewhere in the world. Obviously, the initialization as well as the control of the board must not require a previous training. In fact, it must be a sort of plug & play device. To achieve this topic, the board is controlled by an easy-to-use application using the slow but almost universal RS-232 serial port. This program has been developed in National Instruments Labview® for Windows platforms and in batch-line for Linux/Unix users.

### *D. Adaptability*

The reusability of the test platform can be committed by facts such as the different packages used by the manufacturers. However, in order to avoid a complete new redesign, the system is flexible enough to allow the quick development of a new board test after doing some minor changes, such as the restructuring of the data and address buses, adaptation of the power supply values, etc.

### *E. Reliability*

Usually, the investigation of SEUs in SRAMs consists in writing a pattern in the devices and periodically inspecting if there is a mismatch between the written and read patterns. Unlike DRAMs, SEUs in SRAMs are independent of the written pattern [13]. This fact simplifies the programming of the system since writing the same logic value in all of the cells, either **"0"** or **"1"**, is an acceptable choice.

However, sometimes the process of reading is affected by the external noise or other spurious signals. Therefore, if the system detects a candidate to be an SEU, it rechecks the address three times. Only if the anomalous word is confirmed at least by two readings out of three, does the system accept that an SEU has occurred.

### *F. Radiation Tolerance*

Obviously, the core of a system devoted to study the radiation effects must be itself radiation-tolerant since it will be exposed to the same particles as the memory bank. In order to accomplish this requirement, the system incorporated the following features:

*1) Triple Modular Redundancy, TMR:* A popular way to minimize the radiation sensitivity of custom digital devices is triplicating the system and taking a decision with a voting system. Although this technique increases the size of the design, it guarantees a very high radiation tolerance. However, it is difficult to implement in devices with mixed IN/OUT ports so TMR was not incorporated to the devices with this kind of port.

*2) Resetting:* During the stand-by periods and prior to the writing or reading process, all of the devices except a master receive a reset signal so that they come back to the default state independently of state in which they are. Thus, all of the latent errors present inside the devices are immediately erased. Also, this fact makes easier the design of the HDL code.

*3) NAND Technology:* Xilinx' CoolRunner II CPLDs stores the program in a NAND memory, this technology seeming to be very insensitive to SEUs [7].

Using all these strategies, the possibility of an SEU in the system decision core becomes negligible. In any case, a fourth protection strategy must be incorporated to the system. Instead of sending the data to the computer once the error is detected, the system was programmed to save the data in a backup SRAM memory prior to send the results to the computer. Thus, if the batteries are committed and risk running out of charge, the system reacts checking the memories, saving the results and going to dozing-off state, where the power consumption is

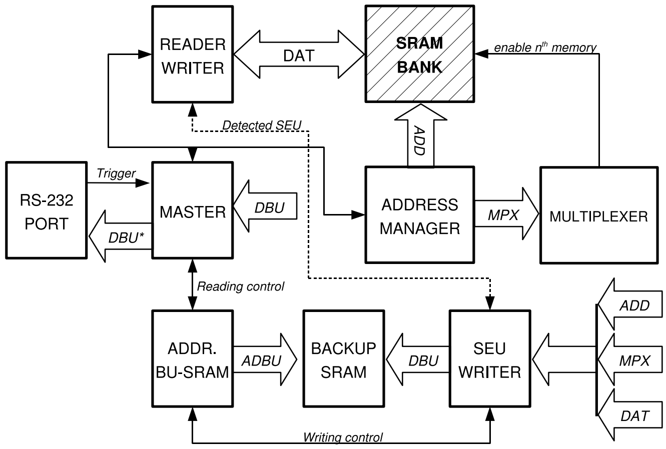


Fig. 1. Internal structure of the device

minimal. However, if an SEU occurs in the backup memory, data can be corrupted so they are registered three times to prevent the incidence of the SEUs.

Finally, although very unlikely, the system is always liable to undergo a catastrophic single event latch-up in some of the SRAM memories. To prevent this fact, the SRAMs are protected by fuses that burn out if such an event occurs. Afterwards, the fuse must be replaced before restarting the experience.

## IV. Description of the Core System

The decision center of the test board is sketched in fig. 1. In the following sections, it will be described in detail.

### A. Main Blocks

In this structure, the following devices can be found:

1) *Master:* The duties of this device are the following: Bridge between the computer and the test board, co-ordination of the other blocks, and reading the back-up SRAM where the summary of single event effects has been registered.
2) *Reader & Writer:* This device has the purpose of writing a reference pattern, which can be selected by the user, in the SRAMs. Besides, it is also devoted to read the data. In case of detecting something odd the process is repeated twice more, and the device weights the data in order to warn the SEU writer against the presence of an SEU.
3) *Address Manager:* The purpose is to select a specific word in the memory bank so that the reader-writer could act on it. The address bus is divided into two sub-buses: The least significant bits are straightly directed to the memory address inputs while the most significant ones go to the multiplexer.
4) *Multiplexer:* As it was previously stated, this device decodes the MPX value and enables only one memory, the others keeping disabled.
5) *SEU writer:* This device starts to work only if the reader-writer communicates that an SEU is confirmed. Then, the system takes the word coming from the memory bank and the whole address and splits the set of data in suitable words to be recorded in the back-up SRAM. This procedure is repeated three times in order to prevent possible SEUs in this SRAM. Another task is to reset the back-up SRAM prior to scanning the memory bank to look for candidates to SEUs.
6) *Addresser of Back-up SRAM:* The purpose of this device is to select a specific address in the back-up SRAM. This address is increased at the request either of the master (reading process) or of the SEU writer (writing process).

### B. Details concerning the practical implementation

The first prototype of the test platform was developed to deal with the 16-Mb CY62167 SRAM memory from Cypress. 64 samples, with a total capacity of 1 Gb, were implemented in the board. This decision imposed some restriction in the selection of the CPLDs. In general, the limitations at the time of implementing the VHDL code configurating the device come from two facts: The number of memory cells to load the code and the number of inputs and outputs. This led to use the XC2C128-VQ100 CoolRunnerII for the master, the address manager and the multiplexer, and the XC2C256-VQ100 for the SEU writer, the addresser of the back-up SRAM and the reader-writer.

### C. Internal System Signals

In the diagram of Fig. 1, the main signals are the following:

- *ADBU:* Address of the back-up SRAM.
- *ADD:* Acronym from ADDress. It is a 20-bit bus to select a specific word inside the enabled memory.
- *DAT:* Data bus registered coming from the memory bank. In the prototype, it was a 16-bit signal.
- *DBU:* Data coming or going to the backup-SRAM.
- *DBU*:* Closely related to DBU. Actually, it is just the DBU after the adaptation to the RS232 protocol, adding the start and parity bits.
- *MPX:* This 6-bit word is used by the multiplexer to select and enable one of the 64 SRAMs of the bank.

Finally, it is necessary to remark that there are other signals that were not included in the diagram. These signals are the *"reset-all"*, coming from the master and leading all of the devices to the stand-by state; the *clocks*, one of both to control the CPLDs and the other one to control the data transmission to the RS232 port; *warning* signals coming from the power supplies to indicate the occurrence of a latch-up or a power failure; finally, the *hand-shaking* signals used by the devices to indicate the others the achievement of the task and, in consequence, that another device must undertake the subsequent task.

## V. Verification Tests

Once the test-platform is built, some mandatory tests are to be done prior to launch a long-term SEE test. First of all, it is necessary to verify that the system correctly operates and, to do that, an auxiliary board had to be developed with the purpose of simulating SEUs. This board sets the reference value during the writing process in such a way that it is constant with exception of some clock cycles, during which the reference value switches. Thus, anomalous values are stored during the writing process, which must be detected in the following reading step. If they were not, bugs must be sought until the system becomes error-free.

Temperature and autonomy tests are also to be done as well as the verification of the absence of alpha-emitter impurities in the devices.

## VI. Ultimate use

As stated in the introduction, the test platform provides data allowing the calculation of the soft error rate of the target SRAM memories. However, the portability of such a platform will allow additional tests such as:

- Distribution of some samples to be used by volunteers around the world with the purpose of verifying if the soft error rate follows the cosmic rays distribution for different latitudes and altitudes.
- Boarding the system in airplanes or stratospheric balloons in order to increase the rate of single events and, thus, to obtain faster test results.

## VII. Conclusion

Field test systems usually suffer from a too large volume that forces the researchers to install them in devoted facilities. However, this paper has shown that the size of one of this systems can be reduced until becoming easily handled and portable.

Along with the portability, the system offers large autonomy to allow a temporary disconnection from the power networks. This fact was achieved by optimizing the design to use only low power device although that meant that large designs, suitable for FPGAs, had to be carefully divided in a set of independent components.

Besides, the system was optimized to face the hazards of natural environments, such as the falls of temperature, radiation, etc. Finally, the system was conceived in such a way that inherited designs from previous tests could be profited to develop a new experiment.

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