Neutron-Induced Single Events in a COTS Soft-Error Free SRAM at Low Bias Voltage

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***Abstract*—This paper presents an experimental study of the sensitivity to 15-MeV neutrons at low bias voltage of advanced low-power SRAMs by Renesas Electronics. The most interesting results are the occurrence of clusters of bitflips, hard errors only visible at low voltage, appearing along with single event upsets. The physical mechanisms are briefly discussed.**

***Index Terms*—COTS, LPSRAM, neutron tests, radiation hardness, reliability, soft error, SRAM**

I. INTRODUCTION

MODERN electronic systems are designed to minimize power consumption. In standby, non-critical devices can be switched off, only keeping connected the main parts of the system to the power supply. However, the information inside CMOS memories is volatile so they cannot be switched off completely. It has been reported that static random access memories (SRAMs) can keep the information even if the bias voltage falls down to 15-20% of the nominal value [1]. Very often, the combinational logic driving the memory cells does not work until the bias voltage returns to the nominal value, but the information does not disappear.

The problem is that, as the bias voltage decreases, the critical charge to trigger a single event upset (SEU) decreases as well. This is also valid for other single events, such as multiple cell/bit upsets (MCU, MBU), etc., with the possible exception of the single event latch-ups (SEL). This fact has led to the demonstration that even electrons, the lightest charged particles, provoke bitflips in 45-nm CMOS SRAMs at ultra-low bias voltage [1].

Recently, a new kind of SRAM has drawn the attention of different research groups. These memories are built by Renesas Electronics in 150-nm CMOS technology and they are called Advanced Low Power SRAMs (A-LPSRAM) [2]. Their main characteristic is that the individual 6-transistor cells are not built in planar technology but in a 3D structure with advantages such as the minimization of the cell area, the incorporation of capacitors that make the occurrence of bitflips more difficult, and the removal of the parasitic *pnpn* structures prone to trigger latch-ups. To the authors' knowledge, the first independent tests on A-LPSRAMs under radiation were performed at the NASA GSFC to investigate heavy ion effects [3]. Recently, the behavior of these memories under very energetic protons has been explored in order to propose its use in the CERN LHC upgrade [4]. Also, the memories were tested under 15-MeV neutrons at the GENEPI2 facility at nominal bias voltage [5].

However, the tolerance of these memories to radiation has not still been investigated in special circumstances, where single events are easier to occur. As it was previously said, bitflips are much more likely to occur when the circuit operates at ultra-low bias voltage, not far from the minimum power supply that allows retention of data. Also, it has been demonstrated that typical static tests underestimate the cross sections so dynamic tests are necessary [6]–[8] for a full understanding of the occurrence of single events.

This paper investigates the behavior of A-LPSRAMs at bias voltages little above the minimum value in static mode, and in dynamic mode. As the first family of tests issued very interesting results, this paper will be devoted to study these phenomena, including new clusters of bitflips and hard errors at low bias voltage.

II. EXPERIMENTAL SETUP

Tests were carried out on one sample of an A-LPSRAM with a capacity of 8 Mbit and configured as 1M×8 bits. According to the manufacturer, the nominal bias voltage ranges from 2.7 to 3.6 V. However, it was verified that even with a bias voltage of 0.60-0.65 V, the information previously written was not lost. Besides, the combinational blocks were operational even with a bias voltage value at least as low as 1.9 V, value below which the read-out system does not work.

A. GENEPI2 neutron source

GENEPI2 (*GEnerator of NEutrons Pulsed and Intense*) is a neutron facility located at the LPSC (Laboratoire de Physique Subatomique et Cosmologie) in Grenoble, France. Since 2013, this accelerator has been used to irradiate integrated circuits from different technologies [5], [9]. It is an electrostatic accelerator producing neutrons by impinging a deuteron beam

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Table I
TIME SEQUENCE OF THE IRRADIATIONS

Round	Pattern	Kind	V_{CC}	Fluence	Affected addresses
A	0×00	Stat.	0.70	2.04	342
B	0×55	Stat.	0.80	2.04	131
C	0×55	Stat.	0.90	2.04	1
D+E	0×55	Stat.	1.00	6.11	0
F	0×55	Stat.	0.70	2.04	130
G	0×55	Stat.	0.75	2.05	338
H	0×55	Stat.	0.85	2.04	312
I	N/A	Dyn.	3.30	0.68	Aborted
J	0×55	Stat.	0.90	4.07	5
K	0×55	Stat.	0.85	2.04	129
L	0×55	Stat.	0.80	2.05	132
M	0×55	Stat.	0.75	2.04	134
N	0×55	Stat.	0.70	2.04	133
O	0×55	Stat.	0.95	6.11	2
P	N/A	Dyn.	3.30	4.28	0
Q	N/A	Dyn.	2.20	4.28	0
			V	$\times 10^9\ n/cm^2$	

onto a fixed target. The target contains either Tritium (T) or Deuterium (D) according to the required neutron energy. After acceleration, deuterons (d) produce neutrons (n) by one of the following fusion reactions: $d + T \rightarrow n + He^4$ and $d + D \rightarrow n + He^3$.

Neutrons are produced with an average energy of either 14.2 MeV for the first reaction or 2.5 MeV for the second reaction. The Devices Under Test (DUTs) are set facing directly the target at a distance determined to match the required neutron flux. Thus, only the most energetic neutrons (15 MeV) hit the device.

Neutron production is monitored throughout the experiments to determine the neutron dose for each irradiation. Early 2015, a fresh tritium target was installed, generating a maximum neutron flux of 4.5 $\times$ 10^7 $n \cdot cm^{-2} \cdot s^{-1}$. Under these conditions, DUTs are exposed to a dose of 1.6 $\times$ 10^{11} $n \cdot cm^{-2}$ within one hour.

B. Test system

The memory was written and read by means of a PIC18F85J90 microcontroller. This device worked with a 20-MHz quartz clock and, experimentally, it was observed that it could work even with a bias voltage of 1.9 V.

In the low-bias voltage static tests, the microcontroller and the SRAM were biased by two independent power supplies. That of the microcontroller was fixed to 3.3 V, and that of the SRAM was tunable from 0 to 3.3 V. SRAM bias voltage was measured with a Keithley 2001 multimeter directly at the memory board. The three grounds (two for the power supplies, and one for the multimeter) were connected near the SRAM board for an accurate measurement. That means that six shielded cables, with a length of 20-m each, were necessary to build the electronic system.

In low-bias voltage static tests, address and data buses, as well as enable signals were set to ground in order to avoid the activation of over-voltage protection structures present in the memories. In consequence, a 0×00 word was always written in the first address in the memory, 0×00000, whichever the pattern was. Let us bear in mind that only 8 bits were sacrificed in a memory with 8 Mbits and, also, it allows testing and debugging the routines to detect the bitflips.

III. RESULTS

As shown in Table I, the tests were performed in successive steps. As there was not any hint to predict the behavior of the memories with ultra-low bias voltages, the irradiations were performed in long steps, next choosing intermediate values, and repeating voltage values at the end of the experiments.

One can see that, at very low voltage values, hundreds of addresses are affected, with single bitflips or MBUs. In general, errors in the irradiations fall in three categories: Clusters of bitflips, hard errors at low bias voltage, and SEUs.

A. Static low bias voltage tests

1) Clusters of bitflips: Irradiations with hundreds of bitflips are characterized by the occurrence of clusters of errors (rounds A-B, F-H, K-N). It is necessary that the bias voltage be 0.85 V or below. Words are corrupted as simple bitflips or events of diverse multiplicity in very close addresses. In particular, the distance between the lowest and highest address of each cluster is around 128. Even more, both boundaries are close to consecutive integer multiples of 128. Table II shows the characteristics of the clusters observed with bias voltage of 0.85 V. In one round, four clusters of different sizes and with error multiplicity up to 7 were registered starting in different addresses and finishing near the end of the address vector. In the other round, the cluster appeared at the beginning of the memory. This fact seems to be universal since clusters never appear in the middle of the memory.

2) Hard errors at low bias voltage: As the tests were performed, it was observed that some addresses reappeared from round to round. For example, it was observed that, from round K and below 0.90 V, the word stored in $0 \times 4D69C$, supposed to be 0×55, systematically changed into $0\times D5$, behavior not observed in the pristine memory. This phenomenon was observed in seven addresses of the memory (Table III). Once the irradiations ended, the memories were checked at the nominal voltage writing different patterns and reading the information, and these addresses seemed to work correctly. However, if the bias voltage falls to 0.7 V, bitflips in the problematic addresses appear again.

A deeper analysis of the results of this table shows that the error in address #6 was not detected during the irradiations since the checkerboard pattern, 0×55, did not change. Besides, errors in addresses #2 and #7 should have been detected in the tests but they were not. Probably, the bit was affected during the last rounds, when dynamic tests at nominal voltages were performed. More interestingly, when the memory was checked one week after the end of the tests, addresses #3 and #4 worked fine. This fact indicates the existence of some kind of physical annealing that mitigates the radiation damage.

These hard errors are roughly similar to the well-known stuck bits, in which the information inside the bit cannot be changed, with the difference that they only occur if there is a cycle of low bias voltage.

Table III
ADDRESSES WITH CORRUPTED INFORMATION AT 0.7 V AND OFFLINE

Written Pattern	Address	Read Word	First Det.	Id.
0×00	$0 \times 4D69C$	0×80	Round K	#1
	$0 \times 8BAE7$	0×08	Offline	#2
	$0 \times 9CE7B$	0×02	Round J	#3
	$0 \times C27AC$	0×80	Round M	#4
	$0 \times EDD7F$	0×80	Round L	#5
$0 \times FF$	$0 \times 31BD9$	$0 \times F7$	Offline	#6
	$0 \times 42FE3$	$0 \times FE$	Offline	#7

3) Single event upsets: Once the bitflips appearing in clusters of errors and those present in different radiation rounds were removed, there was a set of bitflips with characteristics agreeing with those expected in single event upsets: Isolation, randomness, occurrence in only one round, etc. Curiously, this kind of events were not the main contribution to the whole set of errors. For instance, only 4 SEUs were detected combining the two rounds with 0×55 pattern at 0.7 V, the worst-case situation.

Fig. 1 shows the dependence of the SEU cross section with the bias voltage. As the number of errors is not high, error bars are wide and little information can be obtained. At any rate, it seems that the cross section decreases for higher values of the bias voltage, as usually happens in other SRAMs. Above 1 V, no SEUs were observed. Using the procedure explained in [5] and references therein, the conclusion is that the SEU cross section is below $7.2 \cdot 10^{-17}\ cm^2/bit$ for this kind of radiation at $V_{CC} = 1\ V$ with 95%-confidence. This figure beats in more than one order of magnitude the first estimation, $2.0 \cdot 10^{-15}$ cm^2/bit at $V_{CC} = 3.3\,V$, presented in a previous work [5].

B. Dynamic tests

Dynamic tests at 3.3 V and 2.2 V were carried out until reaching a fluence of $4.28 \times 10^9\ n/cm^2$. The latter value was used instead of the threshold one of 1.9 V in order to prevent the microcontroller from slowing down. Read and write operations were performed while the memory was irradiated. In particular, the MARCH-C algorithm was executed [8].

No errors were observed during these tests. As done in Section III-A3, the conclusion is that the cross section is below $1.0 \cdot 10^{-16}\ cm^{-2}/bit$ for this kind of radiation.

IV. Discussion

In a previous work, it was concluded that the SEU cross section in A-LPSRAM memories was two orders of magnitude below those of its counterparts in bulk CMOS technology [5]. However, as other authors have reported SEUs with protons and heavy ions [3], [4], it was likely that SEUs appeared at low values of bias voltage since there is evidence that, at least in bulk CMOS memories, the cross section exponentially grows as the bias voltage approaches the minimum value [10]. Our results show that, indeed, there is an increase in the cross section as the bias voltage gets closer to 0.65 V but, apparently, this growth is not as dramatical as in other memories. Thus, A-LPSRAMs can be safely used with 1-V bias voltage in systems exposed to neutron radiation.

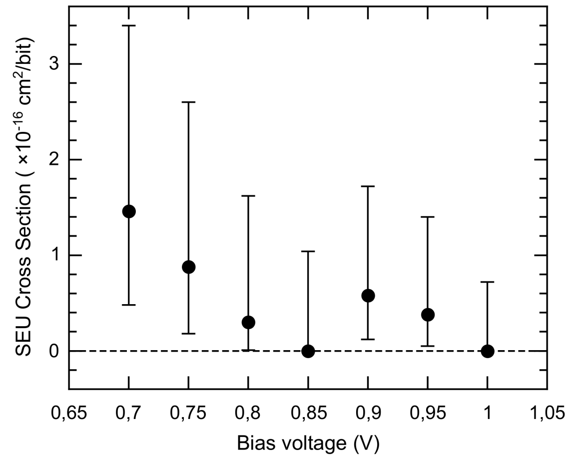

Figure 1. SEU cross section for the A-LPSRAM at ultra-low bias voltage. Error bars were calculated with 95%-confidence.

Another interesting feature of this family of memories is the absence of errors in dynamic tests. As the system was controlled by a microcontroller with a 20-MHz clock, it was not possible to make the SRAMs work near their speed limit as suggested in [7], [8]. However, other SRAMs in 90-nm bulk CMOS technology from another manufacturer showed thousands of events when they were tested in identical conditions to those of the A-LPSRAMs. This good robustness in the dynamic test can be attributed to the absence of physical structures prone to trigger microlatchups. As mentioned in Section I, one of the advantages of the 3D-structure of the A-LPSRAMs is the removal of *pnpn* paths where latch-ups (destructive or microlatchup) originate. According to [7], [8], events with tens of bitflips observed in dynamic tests appear after a microlatchup affecting one of the cell blocks into which the memory is divided. As A-LPSRAM are immune to microlatchups, this phenomenon cannot occur.

Table II
CHARACTERISTICS OF CLUSTERS OF BITFLIPS WITH $V_{CC} = 0.85\,V$

Round	Start	End	Affected addresses	Multiplicity of the events							
				1	*2*	*3*	*4*	*5*	*6*	*7*	*8*
H	$0 \times F9980$	$0 \times F99FF$	94	41	41	10	2	0	0	0	0
H	$0 \times FE982$	$0 \times FE9FF$	55	47	7	0	1	0	0	0	0
H	$0 \times FF180$	$0 \times FF1FC$	35	29	6	0	0	0	0	0	0
H	$0 \times FFF80$	$0 \times FFFFE$	127	2	9	27	34	31	20	4	0
K	0×00001	$0 \times 0007F$	127	1	4	12	26	27	34	17	6

Hard errors at low voltage share some properties with standard stuck bits. Like this well-known hard errors [11], those observed in the A-LPSRAMs vanish days or weeks after the irradiations, and whichever information is written, the bit ends up returning to a stable value. Nevertheless, differences are also evident and this avoids naming them as "stuck bits": Errors keep latent until a low bias-voltage cycle. Also, it is not possible to deduce from the results if the number of errors is proportional to the accumulated neutron fluence.

To the authors' opinion, the hard errors reported in this paper and classical stuck bits share a similar origin: microdose effects [12]. Indeed, it is easy to demonstrate that the CMOS inverters inside a SRAM cell only work if $V_L > V_{THN} + |V_{THP}|$; V_L being the power supply value, and V_{THX} the threshold voltages of the transistors in the inverters. Typically, microdose effects occur with heavy ions but secondary ions generated after the collision of a neutron with silicon nuclei have identical ionizing properties. Therefore, if the threshold voltage of one of the transistors shifts, the minimum bias voltage for the affected cell locally grows. During the low bias voltage cycle, the affected cell is switched off, losing the stored information and when the bias voltage returns to the nominal value, the cell goes to the preferred state after powering up, that can be the same as the original written bit or not. In this last case, a bitflip would be observed.

Due to the absence of information about the way the memories are built, the mechanism leading to the appearance of clusters of bitflips is not fully understood. However, some properties cast light about this phenomenon. First of all, the omnipresence of 128 indicates that the memory may be organized in blocks of 128 8-bit words (1024 bits). Interleaving or error correction codes (ECC) seem to be absent in this memory due to two reasons: The addition of capacitors is a good shield against soft errors so it is nonsense to make the internal organization complicated. Besides, corrupted words in the clusters show events with a multiplicity of up to 8, fact in contradiction with structures with interleaving.

Recent works have demonstrated that clusters of bitflips in bulk CMOS SRAMs are caused by the malfunction of the physical block where the cells are integrated [7], [8]. In this case, the phenomenon is the propagation of microlatch-ups only stopped by the borders of the block. However, in other technologies, latch-ups usually appear only at high values of bias voltage, exactly the opposite behavior observed in the A-LPSRAMs. A-LPSRAMs are supposed to be latchup-free; finally, it was not necessary to switch the memory off to make it working properly again.

One possibility is that, if every block is biased by its own driver, single event transients can lead to a spurious decrease in the bias voltage of the block that erases the stored information. This may explain why clusters do not occur above $0.85\ V$ since even the largest transients would not reach the threshold value to delete the information in the cells. At any rate, other theories can be proposed. It is likely that the row & column decoders play an important but not understood role in this phenomenon. In other memories from the same manufacturer in the range of several Mbits, the datasheets indicate that 7 address bits ($2^7 = 128$) are used for the column decoder, leaving the rest for the row decoder. The abundance of clusters in the addresses between 0×00000 and $0\times000EF$ and around $0 \times FFFFF$ could be related to the fact that the address bus needed to be set to 0×00000 in the experiments. Further work should be done to ellucidate the characteristics of this phenomenon.

V. Conclusions

This paper has presented experimental evidences of the sensitivity to 14-MeV neutrons of an 8 Mbit LPSRAM, manufactured by Renesas Electronics in 150-nm CMOS technology, when powered up at low bias voltage. Interesting conclusions can be drawn from the performed experiments. Results issued from radiation ground tests confirmed that the memory has a cross section below $7.2\times10^{-17} cm^2/bit$ with a 95%-confidence above 1 V. Below that voltage, new kinds of errors were identified: clusters of bitflips in groups of addresses which first and last elements were approximately never more than 128 positions away; and hard errors that were only visible at low voltage, even when the memory is no longer exposed to radiation.

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