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Characterization of Parasitics in Microwave Devices by Comparing S and Noise parameter Measurements with Two Different On Wafer Calibration Techniques

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Abstract* – This paper presents a procedure for an accurate characterization of parasitic effects of terminal pads in microwave devices. This procedure is based on the measurement of S and Noise parameters of the device with two different sets of calibration standards, and simplifies the process of extracting the parasitic elements of the small signal equivalent circuit.

***Keywords* – Microwave, Noise, Calibration.**

I. INTRODUCTION

An accurate characterization of high frequency device parasitics is essential in the development of Monolithic Microwave Integrated Circuit (MMIC) technologies at the level of both device fabrication and circuit design. The degradation of the device performance due to the parasitics can be observed in both the S and noise parameters. The sources of these parasitics in high frequency semiconductor devices can be found in intrinsic deficiencies coming from the own device, as well as from the device terminals. The characterization of microwave transistors such as HEMTs is particularly difficult, since in the small signal equivalent circuit of these devices nearly 50% of all the circuit elements are needed to model parasitics [1].

The extraction of the equivalent circuit of high frequency transistors is usually performed by means of the cold FET method [2]. This method makes it possible to empirically extract all the model elements from S parameter measurements at different bias points. However, it does not provide direct information on the relative contributions to the parasitic effects of the terminal pads.

This paper aims to present a novel procedure to extract information from the origins of microwave transistor parasitics. This procedure is based on the comparison of on wafer S and noise parameter measurements made by using two different calibration kits.

II. RESULTS

In order to study the main contribution to the parasitics in our devices we have performed extensive S and noise parameter measurements in a number of samples covering different gate widths and number of gate fingers. Fig. 1 shows the layout of the investigated devices. The transistors are 0.15 μm gate length devices with gate widths ranging from 4x15 μm to 2x100 μm. These devices were fabricated on a GaAs substrate, and feature a grounded source with a via hole that provides stabilization and facilitates broadband design. In addition, the coplanar terminals facilitate the accessibility of the devices via high frequency probes.

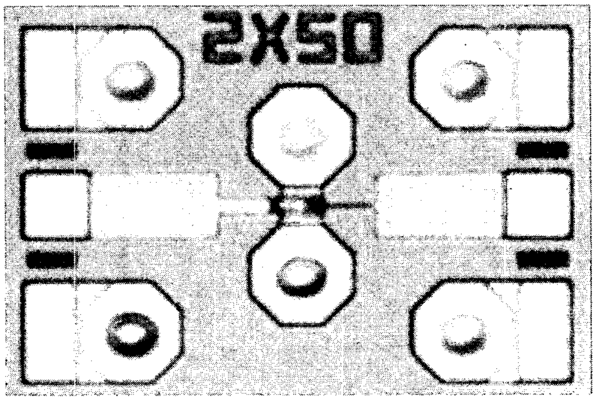

Fig. 1. Layout of a 2x50 μm gate width device

The transistors were designed at Chalmers University of Technology and fabricated at the Philips Limeil Labs [3]. On wafer noise and S parameter measurements were performed in the range 2-26 GHz by using a probe station with a network analyzer (HP8510) and an automated noise measurement system ATN NP5.

Two different calibration kits were used. The first one was implemented in the very same device wafer, as shown in fig. 2. This kit is based on the TRL method [4]. It features two different line standards for broadband calibration and a constant impedance transmission line with two steps for verification. The second one was a calibration kit commercially

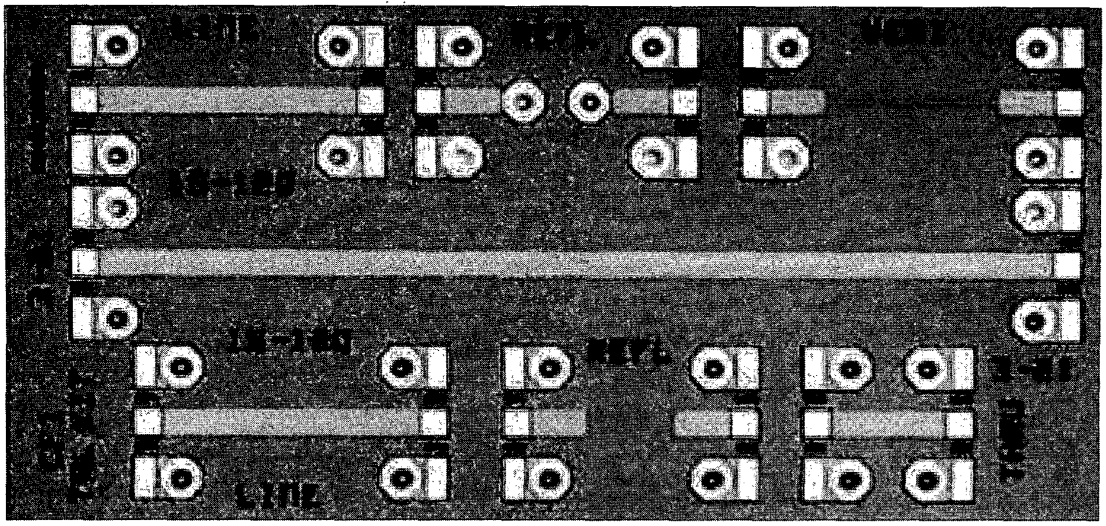

Fig. 2. Implemented calibration kit

available for coplanar probes, fabricated in a ceramic substrate.

The comparison between the measurements performed with the two calibration kits enabled us to investigate the influence of the contact pads, thus obtaining information that can hardly be achieved by means of other procedures. Since the first kit had the same coplanar to microstrip transition than the devices, this kit was the only one which enabled us to effectively remove the influence of the pads. The small signal equivalent circuit was extracted using an in house Lab-View program, which is based in the cold FET approach [5]. The method has been described elsewhere [5], [6].

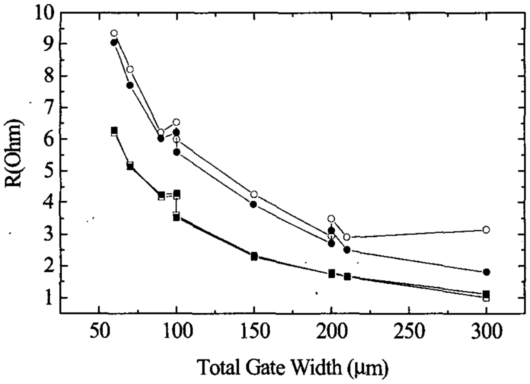

Fig. 3. Influence of the calibration procedure in the extraction of R_s (squares) and R_d (circles). Open symbols: commercial kit. Solid: implemented kit.

Fig. 3 shows the influence of the different calibration procedures on the values of the parasitic drain and source resistance (R_d and R_s). As it can be derived from this figure the main discrepancies are observed in R_s, and directly reveal the contribution of the pad resistance to the total parasitic resistance. In contrast, the values of R_d were not influenced by the calibration procedure, a fact which reveals the weak contribution of the pads to this parasitic resistance.

The use of the implemented calibration kit was especially important in the measurement of the phase reflection coefficient, as it can be observed in fig. 4. The commercial kit led to a noticeable overestimation of this phase even at frequencies as low as 2 GHz. In addition, the use of this commercial kit led to different inaccuracies that were mainly found in the values of the parasitic drain and gate capacitances, which were overestimated in a 300%. This fact can clearly be observed in fig. 5, and is consistent with the overestimation of the optimum reflection coefficient phase previously mentioned. The measurements also showed us that the apparently negligible discrepancies found on the S parameters led to strong discrepancies in the extraction of the parasitic elements of the small signal model, as well as in the calculation of the optimum reflection coefficient for minimum noise figure.

III. NOVELTIES

A new procedure to investigate the influence of the terminal pads in the parasitic elements of a small signal equivalent

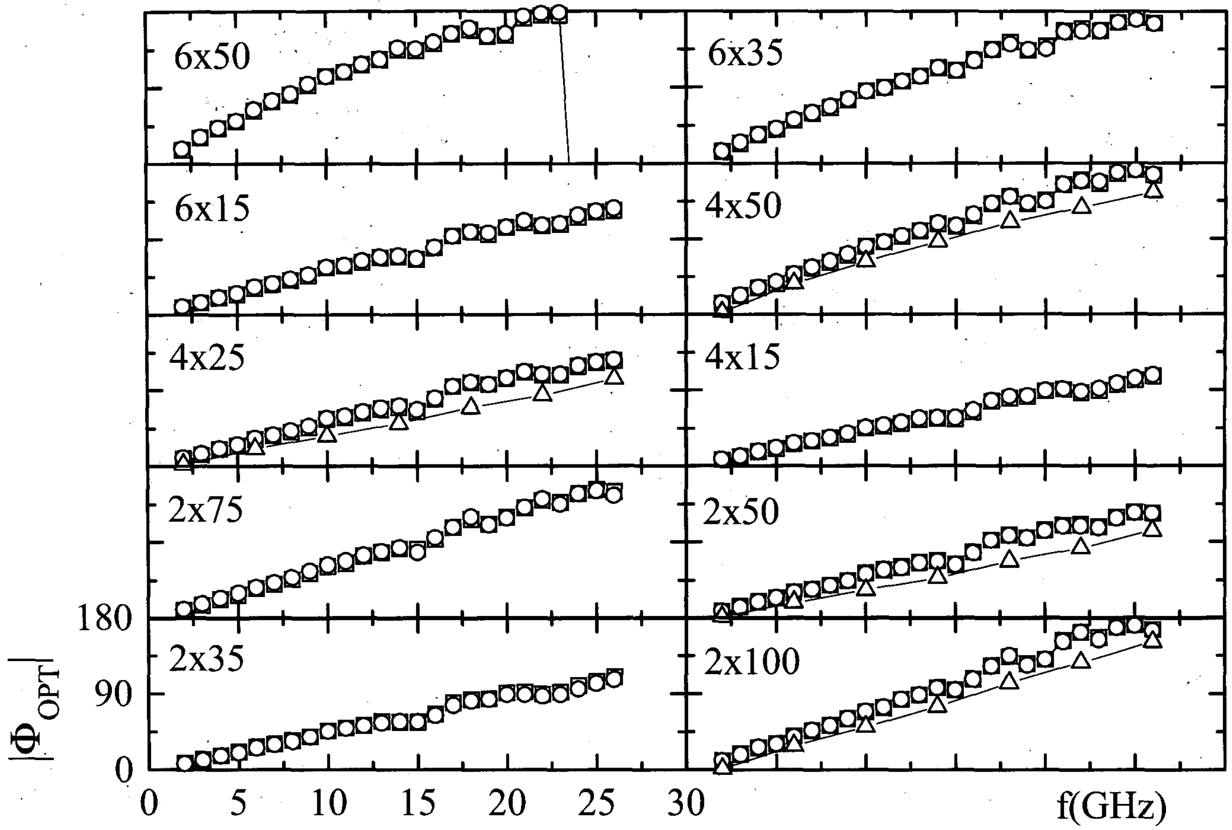

Fig. 4. Influence of the calibration kit on the estimation of the optimum reflection coefficient phase. Squares and circles: commercial kit (two different measurements were made to test the repeatability). Triangles: implemented kit.

circuit of HEMT transistors is proposed here. This procedure is based on the investigation of the discrepancies found in the S and noise parameters measured with two different calibration kits. The method can easily be applied in any commercially available on wafer measurement system, and the ideas on which it is based can also be extended to other microwave devices, such as diodes.

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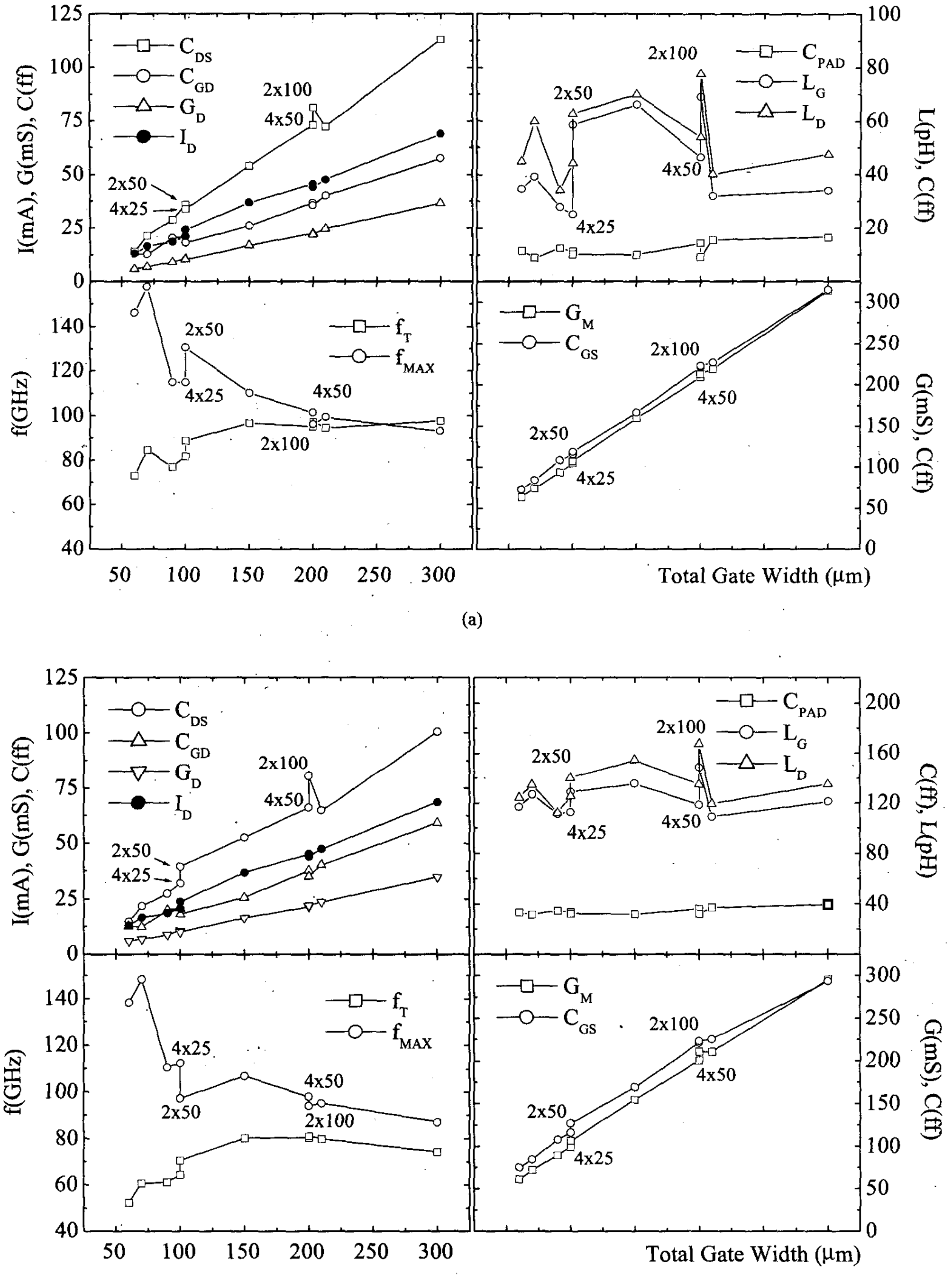

(a)

(b)

Fig. 5. Influence of the calibration kit on the extraction of the parasitic small signal elements. (a) commercial kit. (b) implemented kit. The total gate widths for each point are (from left to right) 4x15 μm, 2x35 μm, 6x15 μm, 4x25 μm, 2x50 μm, 2x75 μm, 2x100 μm, 4x50 μm and 6x50 μm