A LOW NOISE 2-20 GHZ FEEDBACK MMIC-AMPLIFIER

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ABSTRACT

A low noise feedback MMIC-amplifier based on a 180 GHz f_{max} PHEMT-technology is described. The gain, input and output reflection coefficient, dc-power consumption, and noise parameters are investigated theoretically and experimentally as a function of dc-bias and frequency. The noise figure is typically 2.5 dB with an associate gain of 22 dB across the 2-20 GHz frequency range. The circuit area is less than 1μm^2 and the dc-power consumption is lower than 100 mW.

I. INTRODUCTION

For communication, radar, instrumentation, and radiometer sensors there is a need for low noise amplifiers. A versatile building block is the broad-band amplifier and at lower frequencies up to 3 GHz there are commercially available broadband amplifiers based on both Si and GaAs-technologies.

In order to achieve the lowest possible noise figure, the preferred circuit topology is the reflection noise-matched input. However the bandwidth is then limited. For decade broadband amplifiers, the travelling wave concept is often used but the gain and noise performance of this type of amplifier is usually not impressive, the noise figure is of the order 6-7 dB.

The resistive parallell feedback amplifier is an interesting alternative which can yield good input and output match over a large frequency bandwidth. Such amplifier is cascadable for increased gain, and is easily made unconditionaly stable.

In this work, a resistive feedback amplifier is investigated based on a double deltadoped PHEMT-process with 0.1 µm gatelength. The process is available from a commercial foundry [1]. The aim of this work is to investigate possible gain per transistor-stage, dc-power consumption, noise figure, possible obtinable bandwidth, linearity, output power etc as a function of bias. We have measured the bias-dependent noise parameters for individual transistors and extracted parameters for a noise model which can be used in commercial circuit simulators. The design was experimentally verified on MMICs fabricated at the foundry.

II. THE RESISTIVE FEEDBACK AMPLIFIER

The parallel resistive feedback amplifier can be analyzed by ordinary circuit analysis [2]. The relation between transconductance g_m, feedback resistance R_f, and characteristic impedance Z_0 for the condition that S11=S22=0 is

$$R_f = g_m \cdot Z_0^2$$

The gain S_{21} of such an amplifier is then

$$S_{21} = \frac{Z_0 - R_f}{Z_0}$$

The transistor is in this case assumed to be represented by a simple model consisting of only a current generator with transcunductance g_m. The above expression is of course a simplification which nevertheless gives a basic understanding of the underlying principle. In the simulation we use a full equivalent circuit model which also include noise sources.

III. MMIC AMPLIFIER DESIGN

The amplifier was designed to have a minimum gain of 20 dB in a frequency range of 2-20 GHz. In order to achieve this, two transistor stages were cascaded.

The gate and drain of both transistors is in this design are accessable for dc-probes. This enables an independent experimental investigation of the bias-tradeoff between the stages in terms of gain and noise figure.

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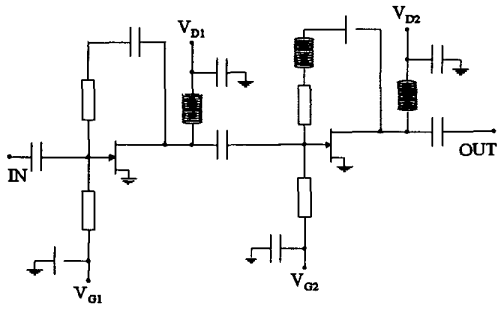

Fig.1 The circuit diagram of the feedback amplifier.

When we know the best bias points, the number of bias-connections can be minimised to only one biasconnection in order to simplify the bias access network. The circuit diagram of the feedback amplifier is shown in the fig 1. Both transistors have a gatewidth of 4x50 μm yielding a transconductance of nominally 160 mS. The feedback network is a resistance of 500 Ω in series with a 2 pF capacitor. The second stage has an inductor in the feedback path in order to give the amplifier a gain boost at the high end of the frequency range. Both drains are connected to the supply voltage through an inductor of value 20 nH. The gates are biased through 250 Ω gate resistors. The input and output are dc-isolated through coupling capacitances. The layout of the MMIC in shown in fig 2. input and output CPW-probes and pads for bias are provided to facilitate 'on wafer' characterization of the amplifier. The total chip area is 2x1.5 mm^2 while the active area of the amplifier is approximately 1 mm^2.

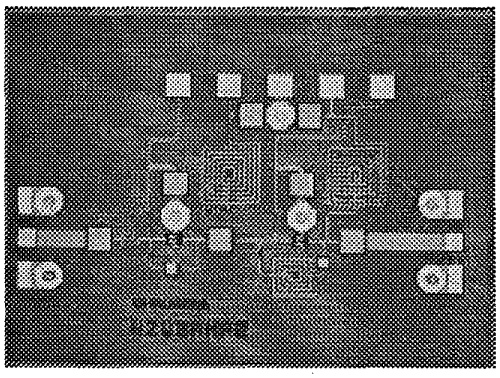

Fig. 2 Photo of the feedback amplifier.

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

The small signal parameters of the devices were obtained by means of the cold-FET method with an equivalent circuit that has been described elsewhere [3]. In addition, the noise parameters of both transistors were measured at different bias conditions. From the noise measurements, the Pospieszalski parameters, drain temperature T_D and gate temperature T_G [4] were initially extracted and then tuned by direct optimization with the gradient method. Once the optimized values were calculated, a non-linear curve fitting was made to obtain an analytical expression for both T_G and T_D as a function of the drain current density. The most accurate prediction of the noise parameters was achieved by assuming a linear dependence for T_G and a hyperbolic dependence with a current density offset for T_D,

$$T_D = T_{D0} \cosh \frac{J_D - J_0}{J_1}$$

Where T_{D0}, J_0 and J_1 are fitting factors. The accuracy of this expression has also been verified at bias points near pinch off operation [5].

Figures 3 and 4 show the calculated drain and gate temperatures for drain voltages of 1 and 2 volts, and different drain current densities. Two transistors of different gate widths were measured to verify the scalability of the model. As it can be observed in figure 3, the discrepancies between the drain temperatures of both devices remain low enough to safely apply the above expression with the same fitting factors to both devices.

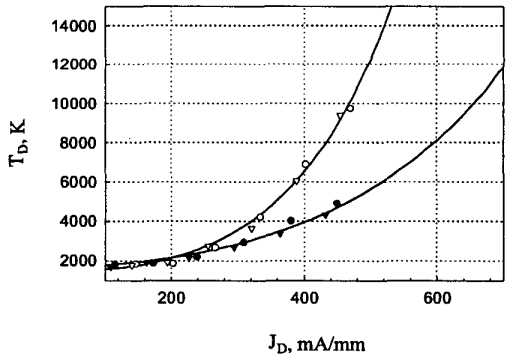

Figure 3. Optimized and fitted (lines) values of the Pospieszalski drain temperature. Circles: transistor with 100 μm and triangles with 200 μm gate width. Open symbols correspond to V_D=2V, solid to V_D=1V.

The MMIC was characterized by a vector network analyzer, HP 8510C, and an "on wafer" noise parameter measurement system (ATN).

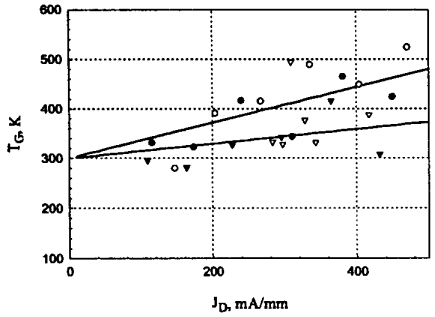

Figure 4. Optimized and fitted (lines) values of the Pospieszalski gate temperature. Circles: transistor with 100 μm and triangles with 200 μm gate widths. Open symbols correspond to V_D=2V, solid to V_D=1V.

The amplifier gain and minimum noise figure (F_{min}) are both given in Fig 5 for the optimum bias conditions. The bandwidth is approximately 20 GHz and the noise figure was about 2.6 dB. Lines represent the simulation made by exploiting a commercially available CAD tool [6]. These simulations could accurately predict both the measured minimum noise figure and gain, and this fact motivated us to investigate the performance that should be expected for a similar amplifier, but designed with a larger first stage transistor (6x50 micron gate width) and a higher feedback resistor (1500 Ohm).

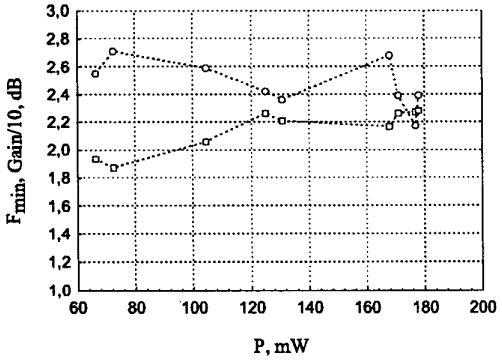

Fig.5 Measured (open symbols) and simulated (lines) minimum noise figure and gain of the wideband amplifier versus frequency. Drain bias of the first transistor V_{D1}=1.5V, for the second V_{D2}=1.5V, gate biases V_{G1}=0V, V_{G2}=0V.

These modifications led to an improved noise figure, 0.2dB less than that obtained in the first design, and also to an slightly higher gain, especially at the lower frequencies.

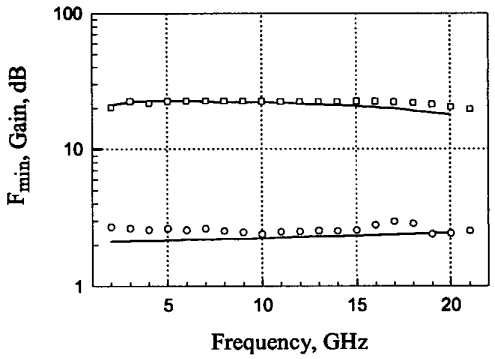

Fig. 6 Measured noise and gain of the amplifier versus power consumption. Open circles stands for F_{min}, open squares – gain/10, dotted line – guide for an eye. The values are taken at 10GHz frequency.

The gain and F_{min} of the fabricated amplifier showed a fairly slight bias dependence. This can be observed in Fig. 6, where the measured gain and noise are both plotted as a function of the dc-power. The best performance of the amplifier is obtained at the 125mW of consumed power, the performance is however acceptable at a power as low as 70 mW. The optimal drain bias was found to be 1.5V for both transistors.

V. SUMMARY

A MMIC broadbandamplifier based on a 180 GHz f_{max} P-HEMT-technology was designed, fabricated and characterized. The amplifier has a gain of more than 20 dB, an input and output reflection coefficient less than -10 dB, a bandwidth of more than 20 GHz and a noise figure of less than 2.7 dB with a dc-power consumption around 100 mW. The simulation of the amplifier noise figure was made by using the Pospieszalski model with unified bias dependent expressions for the drain and gate temperatures. This approach enabled an accurate prediction of the overall amplifier noise performance.

ACKNOWLEDGEMENTS

The Swedish Foundation for Strategic research, SSF, and Chalmers Center for high speed Electronics, CHACH, is acknowledged for the funding of this project.

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