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On the influence of substrate cleaning method and rapid thermal annealing conditions on the electrical characteristics of Al/SiN_x/SiO_2/Si fabricated by ECR-CVD

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Abstract

We investigate the influence of the used cleaning method and rapid thermal annealing (RTA) conditions on the electrical characteristics of MIS devices based on SiN_y:H/SiO_x dielectric stack structures fabricated by electron-cyclotron-resonance plasma assisted chemical vapour deposition (ECR-CVD). We use capacitance–voltage (*C–V*) technique to study charge trapped in the insulator, Deep Level Transient Spectroscopy (DLTS) to study the trap distributions at the interface, and conductance transient (*G–t*) technique to determine the energy and geometrical profiles of electrically active defects at the insulator bulk as these defects follow the disorder-induced gap state (DIGS) model.

1. Introduction

The advent of sub-100 nm technology has led to scale down the dimensions of metal-oxide-semiconductor (MOS) devices. Although the use of amorphous, thermally grown SiO_2 as gate dielectric offers outstanding properties [1], there are several problems when using extremely thin SiO_2 films: interfacial structure, boron penetration, reliability and high leakage gate currents. Stack dielectrics of Si_3N_4/SiO_2 have been described as promising gate dielectrics due to its lower leakage current, reduced boron penetration and higher reliability. Different techniques to grow dielectrics of the Si–O–N family are available [2,3]. Electron cyclotron resonance (ECR) plasma [3] is a very valuable method because it is a low thermal method (implantations may suffer degradations at high temperatures), the substrate is placed outside the plasma chamber free from plasma irradiation or ion bombardment and high activation of the precursor species can be achieved. However, the resultant films are not stoichiometric (Si_3N_4) and some

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hydrogen content is incorporated to the film. These films are usually named SiN_y:H. Prior to the dielectric stack deposition, the substrates must be cleaned. There are several surface cleaning methods, being one of the most important the RCA [4] (Radio Corporation of America) cleaning. It consists of three different steps: First, the Si surface is oxidized, secondly the grown oxide is removed and, finally, the Si surface is oxidized again. The two last steps are sometimes ignored, and that is known as simplified RCA cleaning. After the RCA (complete or simplified), the oxide is removed in HF. Rapid thermal annealing (RTA) treatment is known to improve the insulator/substrate interface, reducing defect concentration. RTA is performed at high temperatures during short times. The aim of this study is to carry out an electrical characterization of SiN_y:H/SiO_x dielectric stack structures: First, a thin layer of SiO_x is deposited by an ECR oxygen plasma oxidation. Secondly, $SiH_{1.55}$:H is deposited by ECR plasma method with SiH_4 and N_2 precursor gases. We investigate the influence of the used cleaning method and RTA conditions on the electrical characteristics of MIS devices. We use capacitance–voltage (*C–V*) technique to study charge trapped in the insulator, deep level transient spectroscopy (DLTS) to study the trap distributions at the interface, and conductance transient (*G–t*) technique to determine the energy and geometrical profiles of electrically active defects at the insulator bulk as these defects follow the disorder-induced gap state (DIGS) model [5].

2. Experimental

2.1. Sample preparation

Two series of MIS devices were obtained as follows: substrates used were n-Si (polished on one side, 5 Ω cm resistivity, 500 μm thick). Before the films were deposited on the substrates, these were cleaned. In the first series, simplified RCA cleaning was carried out, and complete RCA cleaning was carried out in the second series. As complete RCA cleaning consists of three steps, the cleaning in the substrate is deeper than simplified RCA and the roughness of the insulator/semiconductor interface will be smaller. Then, deposition and oxidation processes were conducted in a homemade chamber attached to an ECR Astex 4500 Reactor. High purity O_2 was the precursor gas for plasma oxidation of Si substrate. A 7 nm thick SiO_x is obtained after 60 min plasma oxidation process with a total oxygen flux of 30 sccm. To deposit the SiN_y:H film a mixture of 1.76 sccm of high purity SiH_4 and 8.76 sccm of N_2 was used. The thickness of the $SiN_{1.55}$:H film is 50 nm. At this stage, several series of stacks with the structure $SiN_{1.55}$:H/SiO_x/Si are fabricated. After the deposition is completed, the wafers were cut into several squared pieces (1 × 1 cm) in order to perform the RTA. The differences between MIS devices of each serie is just the RTA temperature. A Modular Process Technology furnace model RTP-600 was used to perform RTA process up to 1000 °C in an Ar atmosphere for 30 s. As-deposited samples were maintained as a reference. Al dots (0.124 mm^2) were electron beam evaporated as gate electrodes. The resultant structure is Al/$SiN_{1.55}$:H/SiO_x/Si/Al. Finally, a post-metallization annealing (300 °C, 30 min, Ar atmosphere) was performed.

2.2. Electrical characterization setup

C–V measurements were carried out at room temperature and at liquid nitrogen (77 K) temperature, putting the sample in a light-tight, electrically shielded box. The measurement setup involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. *C–V* curves are only used to evaluate some features of MIS devices such as flatband voltage and hysteresis phenomena. This technique has been used to determine other features as insulator thickness and interface state density, but in dielectric stacks or in ultrathin layers, the interpretation of the results is different, because *C–V* curves do not fit well with classical models. Deep level transient spectroscopy (DLTS) is a suitable technique to measure interface traps concentrations. Being this technique time sensitive, it allows differentiating contributions with different time constants as fast contributions of interface states and slow contributions corresponding to defects in the dielectric bulk. *C–V* measurements tend to overestimate the interface traps density because it can't separate slow contributions. DLTS measurements, between 77 and 300 K, were carried out using a 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record the capacitance transients. A Keithley 617 programmable electrometer introduces the quiescent bias, and a HP214B pulse generator introduces the filling pulse. To obtain the interface trap distibution within the forbidden gap, the bias voltage is chosen so that the MIS capacitor is just at the limit between depletion and weak inversion. These techniques provide the energy distributions of interfacial states, but do not give information about the spatial distribution. From the experimental conductance transients (*G–t*) measured at different frequencies and at several temperatures, we can obtain the DIGS density as a function of the spatial distance to the interface and of energy positions. Conductance transients are produced by applying bias pulses that drive MIS structures from deep to weak inversion. There are empty DIGS states that can capture electrons coming from the semiconductor conduction band. This process is assisted by tunneling and is time consuming, so states near the interface capture electrons before states located farther away in the dielectric bulk. Conductance transient shape varies with

frequency and temperature because only traps with emission and capture rates of the same order of magnitude than the frequency contribute to the conductance. DIGS state density (N_{DIGS}) is obtained as a function of the spatial distance to the interface and of the energy position as is explained in Ref. [6]. *G–t* measurements were carried out using an HP 33120A arbitrary waveform generator, which apply the bias pulses and an EG&G 5206 two phase lock-in analyzer to measure the instantaneous conductance signal. The conductance transients were recorded by an HP 54501A digital oscilloscope. Temperature ranged from room temperature to 77 K, putting the samples in an Oxford DNI1710 cryostat. An Oxford ITC 502 controller was used to keep the temperature constant during measurements.

3. Results and discussion

Fig. 1(a) and (b) shows capacitance–voltage curves obtained at liquid nitrogen (77 K) for as-deposited and annealed Al/$SiN_{1.55}$/SiO_x/Si/Al capacitors, whose Si substrate has been cleaned by a simplified and complete RCA cleaning, respectively. Fig. 1(a) shows that when simplified RCA cleaning is used *C–V* curves show negative shifts in flat band voltage: As annealing temperature increases the flat-band voltage moves away from the theoretical value (~0.6 V). Negative shifts in flat-band voltage mean that positive fixed charge is being stored in the dielectric bulk. In contrast, when using complete RCA cleaning (Fig. 1(b)), the as-deposited films show the most negative flat-band voltage value and as annealing temperature increase the flat-band voltage shifts towards more positive values, indicating that either positive charges are disappearing from the dielectric or that negative charge compensating the positive one is induced. These results could be explained as follows. Before cleaning, the native oxide, SiO_x, is silicon-rich ($x < 2$). In the case of simplified RCA cleaning, this oxide is not removed during the first oxidation. When performing RTA treatments at temperatures above 600 °C stoichiometric SiO_2 and Si clusters of nanometre size are formed. These clusters are known to be highly defective and induce positive charge in the dielectric. In contrast, when complete RCA cleaning is carried out the native oxide is completely removed during the second cleaning

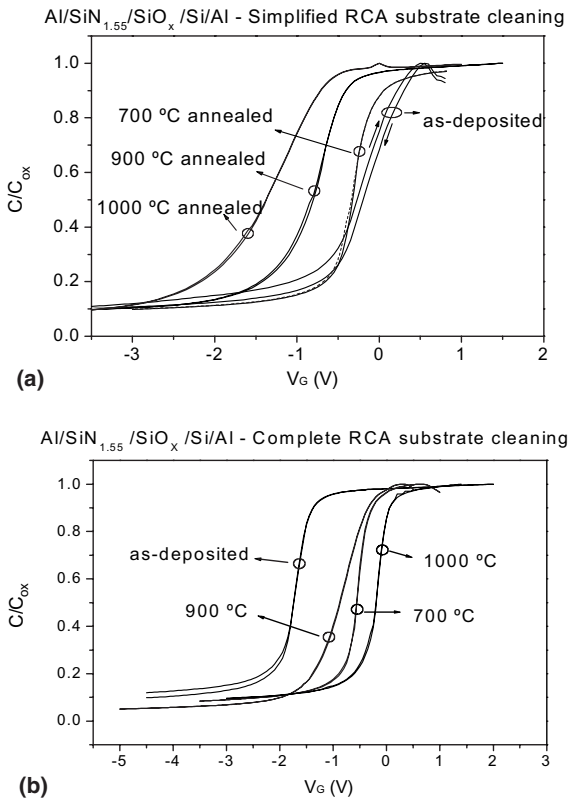

Fig. 1. *C–V* curves for MIS devices annealed at several RTA temperatures and fabricated on simplified (a) and complete (b) RCA cleaned substrates.

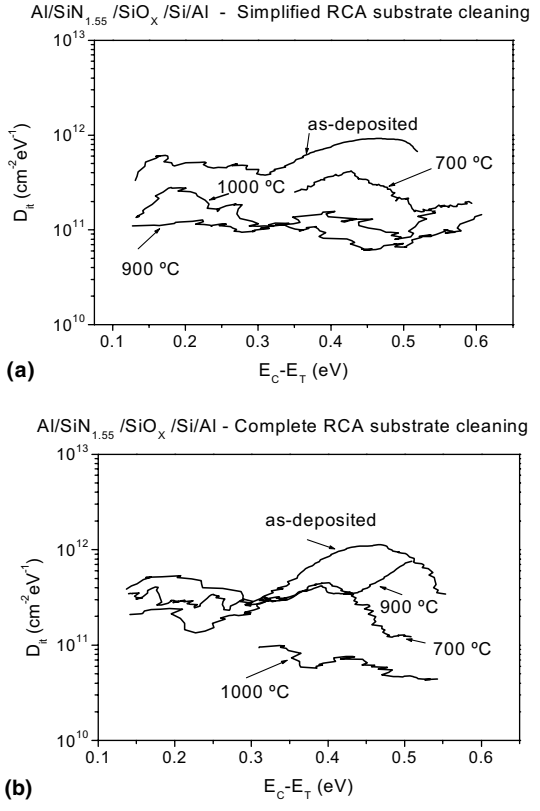

Fig. 2. DLTS profiles for MIS devices annealed at different RTA temperatures and fabricated on simplified (a) and complete (b) RCA cleaned substrates.

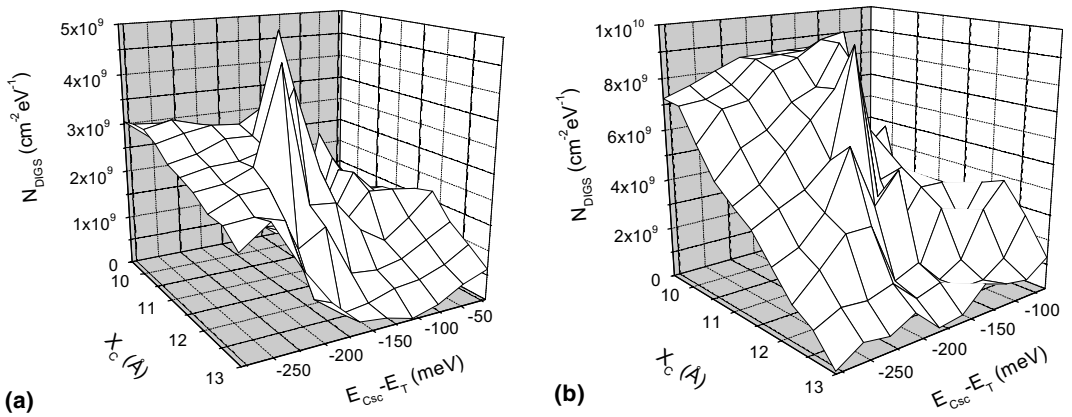

Fig. 3. DIGS profiles for as-fabricated MIS devices fabricated on simplified (a) and complete (b) RCA cleaned substrates.

step. Now, the oxide grown after the final step is oxygen rich and when the samples are RTA annealed the oxygen-rich SiO_x (with $x > 2$) is transformed in SiO_2 and free oxygen ions are moved towards the dielectric inducing negative charge and, therefore, positive flat-band voltage shifts. However, the most important influence of the cleaning method is in the device fabrication yield. When single cleaning is used, the defect clusters can move to the dielectric when annealing and high temperatures yielding no functional devices. Interface-state density profiles have been measured by DLTS. Fig. 2 summarizes the interfacial state density distribution in these capacitors. We can see that in both cases the highest interface trap density corresponds to as-deposited capacitors. When carrying out RTA treatment, interface trap density decreases. In the case of simplified cleaning, the interface trap density is minimum for 900 °C and increases again for an RTA temperature of 1000 °C. Fig. 2(b) shows the profiles obtained for complete RCA cleaned samples. In this case, the lowest interface density corresponds to the 1000 °C annealed sample. In *C–V* measurements, we observe a counter-clockwise hysteresis. This can be due to ejection of electrons from and to the oxide, which indicates that the interface state distribution follows the disorder-induced-gap-states (DIGS): there are defects (slow states) distributed away from the interface to the insulator. We can obtain this distribution by measuring conductance transients, and represent DIGS as a function of the distance to the interface and of the energy position [6,7]. We have measured conductance transients (*G–t*), but the transients were only observed in the as-deposited and in the 700 °C annealed samples. This fact is due to that as annealing temperature increases the defects in the dielectric bulk move to locations farther away from the interface that can not be reached by electrons coming from the semiconductor in measurable transient times. The resultant DIGS plots appear in Fig. 3. In both cases DIGS defects are just over the conduction band, where the electron concentration is very high, so states located near the conduction band have the highest probability for capturing and emitting electrons by tunneling mechanisms. Similar results were obtained for completely RCA cleaned samples.

4. Conclusions

We have investigated the influence of the used cleaning method RTA conditions on the electrical characteristics of MIS devices based on SiN_y:H/SiO_x dielectric stack structures fabricated by ECR-CVD. The cleaning method mainly influences on the yield and reliability of the samples. As for RTA, we have observed noticeable improvements on the interface quality when annealing at high temperatures.

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