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Electrical properties of rapid thermally annealed $\text{SiN}_x\text{:H/Si}$ structures characterized by capacitance–voltage and surface photovoltage spectroscopy

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Abstract

A comparative investigation of the characteristics of the $\text{SiN}_x\text{:H/Si}$ interface has been undertaken by capacitance–voltage measurements and surface photovoltage spectroscopy. By each of these techniques, we have determined the distribution of the interface trap density within the silicon bandgap. The samples were grown by the electron–cyclotron resonance plasma method starting from SiH_4 and N_2 as precursor gases whose flow ratio was varied to produce films of three different compositions: silicon rich, near stoichiometric and nitrogen rich. Post-deposition rapid thermal annealing treatments were applied to observe the evolution of interface properties with the annealing temperature in the range from 300 to 1050 °C. For thin dielectrics, the interface state density has a U-shaped distribution dominated by band-tail states. The minimum of this distribution decreases significantly and shifts to midgap for moderate annealing temperatures. For higher annealing temperatures, the trend is reversed. In the silicon-rich films, the percolation of rigidity caused by the chains of Si–Si bonds impedes the initial decrease of the defect density. For thicker films, the strain of the $\text{SiN}_x\text{:H}$ film produces a higher density of defects that results in increased levels of leakage currents and poorer electrical characteristics.

1. Introduction

In recent years, the continuous down-scaling of the lateral dimensions of field effect transistors below 250 nm has pushed SiO_2 gate dielectrics to their limit of performance by compelling their thickness below the 50 nm range [1]. In this ultrathin regime, direct and Fowler–Nordheim tunnelling currents become comparable to off-state drain currents. In addition, boron atoms from the doped polysilicon gate electrode diffuse through the oxide and pile up at the channel region, degrading the electron or hole mobilities [2, 3]. To counteract such deleterious effects of a reduced oxide thickness, alternative high- k dielectrics, such as $\text{SiN}_x\text{:H}$, have been sought. The use of such dielectric allows a physically

thicker film without reducing the capacitance of the structure and therefore maintaining the necessary transconductance. However, the excellent dielectric properties of thermally grown SiO_2 are difficult to match. While SiO_2 is grown by thermal oxidation of the silicon wafer, therefore forming an almost perfect Si/ SiO_2 interface, $\text{SiN}_x\text{:H}$ films should be deposited by chemical vapour deposition (CVD) techniques. This results in a defective interface in which the high density of interface traps blocks the modulation of the channel conductivity.

As the process temperature becomes important in order to avoid the redistribution of dopants out of implanted areas, plasma-activated techniques are necessary to reduce the heating of the substrate during the growth of the film. When the deposited $\text{SiN}_x\text{:H}$ film is used for passivation or isolation pur-

poses, direct plasma excitation may be a satisfactory solution. However, the exposure of the growing surface to direct bombardment of ions from the plasma causes a high density of interface defects and makes the SiN_x:H dielectric useless for gate applications in field effect devices. Hence, indirect plasma methods become necessary. Among them, the best results have been obtained by the remote plasma enhanced CVD process (r-PECVD), developed by the North Carolina State University group, [4, 5] and by the electron–cyclotron resonance (ECR) method [6–10]. An advantage of the ECR method against the r-PECVD process is that ECR presents higher ionizing efficiency. This allows the use of N₂ as the precursor gas in SiN_x:H deposition, while in the r-PECVD plasma system hydrogen-containing ammonia (NH₃) must be used.

SiH₄ is used as the precursor gas of Si atoms in both the r-PECVD and the ECR plasma methods. Due to the low deposition temperature, part of the hydrogen atoms of the excited fragments of SiH₄ generated in the plasma region are incorporated to the growing SiN_x:H film. For the r-PECVD plasma system, an additional source of hydrogen comes from the NH₃ molecule used as a precursor of the nitrogen atoms. Therefore, for the same nitrogen to silicon ratio and deposition temperature, the content of hydrogen of the films obtained with the r-PECVD plasma method is usually significantly higher than the corresponding ECR films. The amount and distribution of the hydrogen content is of fundamental importance for determining the electrical properties of the SiN_x:H film.

Additionally, the response of the dielectric to post-deposition thermal treatments is also largely determined by the bonding configuration of the hydrogen atoms. Rapid thermal annealing (RTA) processes have been used with success to improve the electrical characteristics of SiN_x:H films. In the case of films with high hydrogen content (this is the case of the r-PECVD) the best results are obtained at high annealing temperatures (900 °C). The reason seems to be the bonding reconstruction that takes place when N–H and Si–H bonds are thermally broken producing the effusion of hydrogen molecules and Si–N bond healing [11, 12]. In contrast, for SiN_x:H films deposited by ECR, most authors agree that the best annealing temperature is around 600 °C or even lower [13]. In this case, it seems that the effects of the RTA treatments are associated mainly with the thermal relaxation of bonding constraints. The dehydrogenation processes that take place at higher temperatures have a negative effect because they are not accompanied by bond reconstruction due to the lower flexibility of the network, which in turn is associated with a lower hydrogen content [14].

In previous articles, we have analysed in detail the evolution of the bonding structure of ECR plasma deposited SiN_x:H films of variable composition, subjected to RTA post-deposition treatments at temperatures ranging from 300 to 1050 °C [15–17]. A further study showed that the electrical properties of the SiN_x:H/Si interface should be analysed in conjunction with the defect structure of the material, i.e. with the presence within the SiN_x:H bulk and at the SiN_x:H/Si interface of the so-called Si dangling bonds [14, 18].

In this paper, we present a new investigation on the electrical properties of these devices. We analyse the SiN_x:H/Si interface by the capacitance–voltage (*C–V*) and surface photovoltage (SPV) techniques.

The SPV technique has been used to obtain the distribution of trap states on the Si surface after different chemical treatments [19, 20]. Additionally, the interface of elemental and compound semiconductors with native oxides [20, 21], the Si/SiO₂ interface [22], the Si/glass [23] interface and compound semiconductor–metal interfaces [24] have been analysed with this technique. Finally, the SPV method has also been used to determine the surface recombination velocity of semiconductors [25]. Up to now, we have not found any application of this method to the investigation of interface states of the relevant SiN_x:H/Si interface. The work presented in this paper tackles this issue from a comparative point of view. We will obtain the density of interface states from the SPV method and we will compare the results with the same parameter determined from *C–V* measurements.

Compared with the *C–V* method, the SPV technique has the advantage of being non-destructive. This is especially useful for monitoring the characteristics of a device through successive fabrication steps. Other important advantages are the tolerance to slightly non-ideal dielectric layers (pinholes, roughness, etc...) and to relatively thick films which are otherwise difficult to characterize by *C–V* measurements.

2. Experimental

The devices analysed were SiN_x:H thin films obtained by the ECR plasma method deposited on silicon substrates, which were heated at 200 °C during the deposition process. The reactor was an Astex 4500 machine operated at 100 W of microwave power and 0.67 mTorr of process pressure. Three types of films were deposited whose composition was controlled by the flow ratio of the precursor gases, which were N₂ and SiH₄. The ratio $R = N_2/SiH_4$ was found to be the deposition parameter that most influences the composition, both the proportion of nitrogen to silicon ($x = N/Si$) and the hydrogen content of the films [26]. The three types of films were obtained with the following values of the gas flow ratio:

- (1) Films deposited at $R = 1$, result in a silicon-rich (Si-rich) composition with $x = 0.97 \pm 0.03$ and hydrogen bonded predominantly to Si.
- (2) Films obtained with $R = 1.6$ give $x = 1.43 \pm 0.02$ and a minimum content of hydrogen among the three types of film. This type of film will be referred to in what follows as near-stoichiometric.
- (3) Finally, films deposited at $R = 7.5$ produce nitrogen-rich samples (N-rich) with $x = 1.55 \pm 0.04$ and hydrogen bonded only to N.

The n-type Si wafers were (100) oriented and had a 5 Ω cm resistivity. They were cut into square pieces of side length 5 mm before growing the samples. After this, they were subjected to a cleaning procedure, based in organic solvents and dilute HF, inside a purged glove chamber directly coupled to the entrance port of the vacuum chamber.

Post-deposition RTA treatments of 30 s were applied to different samples at temperatures from 300 to 1050 °C. The RTA furnace was a Modular Process Technology RTP-600 machine in which the samples were placed inside a closed graphite susceptor located in a sealed quartz chamber purged with Ar gas. To ensure maximum consistence of

the results within each sample series, nine identical films of each composition were deposited in the same run, so that the samples annealed at different temperatures had been grown simultaneously under identical conditions.

The thickness of the samples was a crucial factor in this work because of the inherent stress of the $\text{SiN}_x\text{:H}$ films. The strain of the $\text{SiN}_x\text{:H}$ lattice increased with its thickness causing a higher density of defects both in the bulk and at the interface, and consequently an increase of leakage currents which made impossible the measurement of the quasi-static capacitance for films thicker than about 100 nm. For this reason, we chose to analyse separately two sets of films. The first set was formed by samples of reduced thickness, some of which were investigated by SPV and others by C - V measurements. The second set was of thicker samples characterized only by SPV. In the reduced thickness case, the samples that were characterized by C - V measurements had to be contacted with metal electrodes. This was done by thermal evaporation of Al. No contacts were needed for the SPV measurements.

A detailed description of the SPV setup can be found in [23], and the physical foundation of the method is explained in [27]. Basically, the measuring procedure is as follows: a laser pulse impinges on the $\text{SiN}_x\text{:H/Si}$ structure through a transparent upper contact (TCO: transparent conducting oxide), made of ZnO, and a mica spacer. The light pulse passes through the $\text{SiN}_x\text{:H}$ and generates electron-hole pairs at the silicon surface. The electric field in the space charge region separates charge carriers of opposite sign, and consequently flattens the band bending. This is observed as a change of potential at the electrode. The photovoltage pulse decays exponentially as the charge carriers recombine and the semiconductor returns to equilibrium. Then a different bias is applied to the TCO contact and the measurement is repeated. In this way, a relation between the applied potential and SPV is obtained. The interface trap density (D_{it}) at the $\text{SiN}_x\text{:H/Si}$ interface obtained from the SPV method is given by

$$D_{it} = -\frac{1}{q} \frac{dQ_{ss}}{d\phi_s}, \quad (1)$$

where Q_{ss} is the charge trapped in interface states, q is the charge of an electron, and ϕ_s is the potential at the semiconductor surface. Considering the relation between charge variations at the gate electrode (dQ_g), space charge region (dQ_{sc}) and interface states (dQ_{ss}), and an analogous relation between the gate voltage (dV_g), surface potential ($d\phi_s$) and voltage drop (dV_0) in the two dielectrics (mica plus $\text{SiN}_x\text{:H}$), one arrives at the following equation for the density of interface states:

$$q D_{it} = \frac{dQ_g}{dV_0} \left(\frac{dV_g}{d\phi_s} - 1 \right) + \frac{dQ_{sc}}{d\phi_s}, \quad (2)$$

where dQ_g/dV_0 is the capacitance of the series of the two insulators (a known parameter), $dQ_{sc}/d\phi_s$ is the capacitance of the space charge region of the semiconductor, which can be calculated for each value of ϕ_s if the doping is known, and $dV_g/d\phi_s$ is the experimentally determined parameter, since the measurement procedure provides us with a dc relationship between gate voltage and surface potential. Here it is commonly assumed that the illumination flattens the bands

completely, so that the surface potential is obtained directly from the saturation photovoltage. However, we have not used this assumption, and additionally we have taken into account the so-called Dember effect. The complete expression that relates the band bending and the photovoltage taking into account the Dember effect and the non-saturation conditions can be found in [19].

We have also characterized the $\text{SiN}_x\text{:H/Si}$ interface by means of C - V measurements. The high-frequency (1 MHz) and quasi-static capacitance were measured simultaneously with a Keithley Model 82 system on samples on which Al electrodes had been applied by thermal evaporation. From the equivalent circuits of the metal-nitride-silicon (M-N-S) structures in accumulation, depletion and inversion, the contribution of the interface traps to the capacitance (C_{it}) at low frequencies can be calculated according to the well known expression (see [28])

$$C_{it} = \left(\frac{1}{C_q} - \frac{1}{C_{diel}} \right)^{-1} - \left(\frac{1}{C_h} - \frac{1}{C_{diel}} \right)^{-1}, \quad (3)$$

where C_q is the quasi-static capacitance, C_h is the high-frequency capacitance, and C_{diel} is the capacitance of the dielectric. This expression is correct only in the accumulation and depletion regions. In inversion, the results will be affected by the additional error that introduces the inclusion of the inversion capacitance within the trap capacitance.

The interface traps capacitance can be related to D_{it} using the commonly accepted approximation where the integral of D_{it} times the differentiated Fermi function over the gap is replaced by D_{it} (for more details, see [28]):

$$C_{it}(\psi_s) \approx q D_{it}(\psi_s). \quad (4)$$

Here ψ_s is the band bending in the semiconductor and ϕ_s is the position of the Fermi level at the interface with respect to the intrinsic Fermi level, that is to say, the surface potential. Therefore equation (4) relates the measured capacitance $C_{it}(\psi_s)$ with the density of traps $D_{it}(\phi_s)$ around an energy level inside the gap located next to the Fermi level. Following again [28], the value of D_{it} can be positioned correctly within the gap from the known values of the band bending (ψ_s) and the bulk doping level (ϕ_B).

In the following, the interface trap density will always be denoted as D_{it} , whether this parameter was obtained by the SPV method or with C - V measurements.

3. Results

We shall divide the study in two sections: thinner samples i.e. samples that were analysed by both C - V and SPV techniques, and thicker samples, investigated only by SPV. In the first part we studied thinner samples of the three compositions discussed in the experimental section. The samples for SPV had an as-grown thickness of 40 nm and had no metal electrodes. The samples for C - V measurements were of 40 nm thickness for the $x = 0.97$ and $x = 1.43$ compositions and 30 nm thickness for the $x = 1.55$ case.

In the second part, thick films of the near-stoichiometric and N-rich compositions were analysed. We deposited two sample series of thickness 130 nm in the first case and 100 nm in the second.

Figure 1. High-frequency (solid curves) and quasi-static (dotted curves) capacitance versus gate voltage for three devices made with nitrogen-rich films. The first device (upper graph) had no RTA treatment, while the other two were treated at the temperatures indicated in the figure. Dashed vertical lines mark the flat band voltage.

3.1. Thin samples

In figure 1 we plot the result of C – V measurements before and after RTA processes at 600 and 800 °C for a $\text{SiN}_x\text{:H/Si}$ structure in which the $\text{SiN}_x\text{:H}$ layer was N-rich. The flat band voltage is also shown in this figure. It is observed that the dip of the quasi-static capacitance is enhanced by the annealing at 600 °C, indicating a reduction of D_{it} at the interface. When increasing the annealing temperature above 600 °C the device deteriorates, causing a high value of D_{it} and an increase of leakage current through the dielectric. Consequently, the dip of the quasi-static capacitance is less significant. Such behaviour can be appreciated in the third graph of figure 1, corresponding to the 800 °C RTA. In the latter plot, the increase of the quasi-static capacitance when the polarization enters the inversion region is due to the increase of leakage current through the $\text{SiN}_x\text{:H}$.

For the near-stoichiometric films, the behaviour is qualitatively similar to the one described above, except that now the temperature at which minimal deviation occurs between the high-frequency and quasi-static curves in depletion is 400 °C. The highest temperature that the dielectric can stand with a leakage current low enough to make possible the measurement of the quasi-static capacitance is 700 °C.

In the Si-rich sample, there is no significant change of the depth of the quasi-static dip at any annealing temperature. Instead, the depletion region progressively becomes shallower with increasing annealing temperature in the whole range of RTA treatments, until no quasi-static capacitance can

Figure 2. High-frequency (solid curves) and quasi-static (dotted curves) capacitance versus gate voltage of devices based on Si-rich films. The vertical dashed line is the flat band voltage.

be measured above 500 °C. Figure 2 compares the C – V characteristics of the sample annealed at 500 °C with the one that had not undergone any RTA process.

Figure 3 shows the results of D_{it} obtained from C – V measurements for several films of the three compositions and different annealing temperatures. In the N-rich series, the minimum of D_{it} decreases by a factor of three (from 3.6×10^{11} to $1.2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$) when the device is subjected to a RTA treatment at 600 °C. An analogous reduction takes place in the near-stoichiometric samples, which experience a decrease from $4 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ down to $1.2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ in the sample treated at 400 °C. The reduction of D_{it} in the moderate range of annealing temperatures is accompanied by a shift of the minimum of D_{it} towards midgap, which results in a more symmetric U-shaped curve. For annealing temperatures higher than those ones, D_{it} increases sharply in both the N-rich and near-stoichiometric films.

In the Si-rich composition the interface deteriorates upon annealing at any temperature, there being an increase of D_{it} and a narrower U-shaped distribution.

The minimum of D_{it} is commonly used to assess the quality of an insulator–semiconductor interface. Figure 4 shows the values of this parameter versus RTA temperature for the three compositions of the $\text{SiN}_x\text{:H}$ films. In this figure, we observe that in the N-rich and near-stoichiometric samples, the minimum of D_{it} decreases up to an intermediate temperature (600 °C in the first case and 400 °C in the second). This is not observed in the Si-rich case, which experiences a moderate increase of the minimum of D_{it} up to the temperature in which the quasi-static capacitance can no longer be measured (above 500 °C).

There is an interesting parallelism between the trends of D_{it} for each type of film and the analogous trends followed by bulk defects in the $\text{SiN}_x\text{:H}$ measured by electron spin resonance (ESR). Comparative graphs for each composition

Figure 3. Density of interface states referred to midgap energy obtained from the C - V curves for the N-rich samples (upper graph), near-stoichiometric samples (middle graph) and Si-rich films (lower graph).

Figure 4. Values of the minimum of the density of interface states as a function of the RTA temperature. The results correspond to the three types of $\text{SiN}_x\text{:H}$ films studied in this work, whose composition is identified in the figures. The curves are guides to the eye.

are shown in figure 5. The ESR results have been discussed in detail in previous publications [14, 18]. They were obtained on samples deposited under identical conditions as those analysed in this paper. Here we will only remark upon the analogy between the trends of the densities of bulk defects (silicon dangling bond centres, N_{db}) and D_{it} . For the N-rich samples (upper graph of figure 5) both parameters follow parallel trends, with a minimum at around 600 °C. Therefore this is the optimum annealing temperature. In the near-stoichiometric case, N_{db} also has a minimum at 600 °C, while D_{it} has its lower value at 400 °C. Finally, the trend for N_{db} in the Si-rich samples is almost flat up to 800 °C. The minimum value

Figure 5. Density of interface states (open symbols) compared to Si dangling bond density (full symbols) as a function of annealing temperatures for the three $\text{SiN}_x\text{:H}$ compositions: N-rich (upper graph), near stoichiometric (middle graph) and Si-rich (lower graph). Curves are drawn as a guide to the eye.

occurs at 400 °C, but using the same scale for the graphs of the three compositions, as in figure 5, we see that this minimum is much less significant than for the other two cases. Furthermore, D_{it} has no minimum for this composition and it can only be measured up to 500 °C, showing a slightly increasing trend.

In addition to D_{it} , the C - V measurements provide information about the effective charge in the insulator, and also about the density of slow traps located in the vicinity of the silicon substrate. Both parameters are obtained from the flat band capacitance. The first one is calculated directly taking into account the contribution of the work function difference to the shift of the capacitance curve. The second one is evaluated from the hysteresis of the high-frequency capacitance between two consecutive sweeps from accumulation to inversion and vice versa. Although the information contained in both parameters is not exactly the same, both are related to charge trapped inside the $\text{SiN}_x\text{:H}$ layer, in contrast to D_{it} , which is related to interface defects. In figure 6 we plot the value of the hysteresis as a function of the RTA temperature. The three types of films show a significant decrease of the hysteresis when the temperature of the RTA is increased. In the N-rich and near-stoichiometric samples, the hysteresis practically disappears for annealing temperatures above 600 °C. In the Si-rich films, a significant hysteresis remains even for the higher annealing temperature.

The data plotted in figure 6 reveal the quite different origin of the defects responsible for charge capture in the $\text{SiN}_x\text{:H}$ compared to D_{it} and N_{db} . In the discussion section we will

Figure 6. Hysteresis as a function of the RTA temperatures. Curves are a guide to the eye.

Figure 7. Density of interface states referred to midgap energy, obtained from the SPV method. For each composition, the results corresponding to the most significant annealing temperatures are shown.

analyse in detail this discrepancy and propose a model for each type of defect.

The results of the calculation of D_{it} from the $C-V$ curves were largely confirmed by the SPV study. Figure 7 shows the D_{it} distribution obtained from the SPV method for several annealing temperatures of the three compositions. This graph should be compared with figure 3, where the same parameter obtained from the $C-V$ curves was shown. Clearly, the same trends are reproduced in the results of SPV. In the N-rich films the distribution becomes wider, more symmetric and with a lower minimum at the annealing temperature of 500 °C. In the near-stoichiometric samples the same effect takes place with the RTA process at 400 °C, but surprisingly, and in

Figure 8. Minimum of the interface state density as a function of the RTA temperature for all samples analysed. Solid symbols: obtained from the SPV method. Empty symbols: values given by the $C-V$ measurements. Curves are drawn to guide the eye.

contrast to what was observed in the $C-V$ measurements, it is maintained in the RTA treatment at 700 °C. Finally, in the Si-rich composition, low values are maintained at moderate temperatures, but without a clear improvement, in much the same way as it occurred with the results of the $C-V$ measurements. For higher annealing temperatures, the interface deteriorates in the three cases, showing an increase of D_{it} and narrower and less symmetric distributions. Some tendency to Fermi level pinning is observed at 900 °C for the nitrogen-rich composition and at 700 °C for the silicon rich films. Comparing with the values of D_{it} given by the $C-V$ method, the SPV produces concordant results in general, except for the aforementioned difference in the near-stoichiometric series.

In order to facilitate the comparison between the results of both methods, we plot in figure 8 the minimum values of D_{it} for each annealing temperature of the three types of films, obtained by the $C-V$ and SPV methods. The Si-rich films show an excellent agreement between the results obtained by the two different methods. For temperatures higher than 500 °C there are no values corresponding to the $C-V$ technique because the quasi-static capacitance cannot be measured. In the near-stoichiometric and in the N-rich samples, the values obtained by SPV are generally a bit higher than those of the $C-V$ measurements, although both results are within the same order of magnitude. Additionally, in the N-rich series the trends are exactly parallel in the lower range of annealing temperatures and tend to join for higher temperatures. Some discrepancy appears in the near-stoichiometric films, as commented above concerning figure 7. The SPV results show that the beneficial effects of the RTA treatments endure for annealing temperatures up to 700 °C,

Figure 9. Photovoltage (V_{ph}) versus bias voltage characteristics (left-hand side) and distribution of interface states versus energy (right-hand side). The data correspond to a set of thick samples (100 nm) of a N-rich composition.

Figure 10. Photovoltage (V_{ph}) versus bias voltage characteristics (left-hand side) and the distribution of interface states versus energy (right-hand side). The data correspond to a set of thick samples (130 nm) with near-stoichiometric composition, subjected to different RTA treatments. As can be observed, the inversion region is not reached. Also, a peak appears in the D_{it} distribution that shifts to lower energies with increasing the annealing temperature.

while the damage begins at higher temperatures (see also figure 7). This is not in agreement with the trend shown by the minimum of D_{it} obtained from the $C-V$ characteristics, as can be clearly appreciated in the middle graph of figure 8.

3.2. Thick samples

We only studied the two compositions that gave the best results as a function of the annealing temperature, that is to say, the N-rich and near-stoichiometric. As we detail in the experimental, the thicknesses of the $\text{SiN}_x\text{:H}$ films were 100 nm (N-rich films) and 130 nm (near-stoichiometric). That means about three times the thickness of the samples used for the study considered in the previous section. The first consequence of increasing the film thickness is that important leakage currents appear through the dielectric when a polarization is applied, making impossible the measurement of the quasi-static capacitance. For this reason, the interface can only be investigated by the SPV method.

In figure 9 we show the results that we have obtained for the N-rich films. Both the photovoltage versus bias voltage and D_{it} are shown. It is interesting to visualize both curves together because the relation between them becomes clearly apparent: once the photovoltage is converted to surface potential, D_{it} is obtained from its derivative according to equation (2). For

this reason, the steeper the transition of the photovoltage from accumulation to inversion or vice versa (i.e. the higher the slope of the plots on the left-hand side of figure 9), the lower D_{it} will be. Qualitatively, the evolution that this parameter shows with annealing temperature is similar to what was reported for the thin samples in figures 7 and 8. In this case 600 °C is the optimum annealing temperature, since it presents the wider, lower, and more symmetric distribution of D_{it} together with the more abrupt transition of the photovoltage curve between accumulation and inversion. Therefore, the evolution of the interface characteristics with annealing temperature is essentially the same as in the thin samples. However, the value of the minimum of D_{it} is about a factor two higher in the thick samples. This is the consequence of the stronger strain brought to the interface by the stress of the higher thickness of the $\text{SiN}_x\text{:H}$ layer.

Performing a similar joint analysis of photovoltage curves and D_{it} distributions for the near-stoichiometric thick samples gives quite different results. We illustrate this case in figure 10. The only graphs that appear complete are the ones corresponding to the untreated sample. The other ones are truncated because the polarization sweep cannot be wide enough (our experimental setup was limited to ± 1000 V). Therefore, the photovoltage curves are interrupted without reaching the upper region in which the slope would tend to zero

indicating the approach of the Fermi level to the valence band. Consequently, D_{it} cannot be calculated in the respective region below midgap. It is also striking to find the appearance of a peak in the D_{it} spectra of the annealed films. The position of this peak has been marked by an arrow in the figure and it shifts to lower energy values with increasing annealing temperature. The peak corresponds to a feature in the photovoltage curve (the flattening of this curve) which is especially noticeable for the two higher annealing temperatures. In the next section, we will discuss its possible origin.

4. Discussion

4.1. Thin samples

We will focus the discussion on the minimum of D_{it} , since it is considered as the most relevant indication of the quality of the interface. The representative C – V measurements of figures 1 and 2 led to the D_{it} distributions of figure 3. For the near-stoichiometric samples, the C – V curves were omitted because of the complete similarity with the N-rich case plotted in figure 1. These distributions should be compared with those obtained by SPV and shown in figure 7. We observe two different types of trends with annealing temperature. On the one hand, the N-rich and the near-stoichiometric films have an optimum annealing temperature in which the sweep of the Fermi level is wider and D_{it} is lower. This temperature is 600 °C for the N-rich series and 400 °C for the near-stoichiometric.

With regards to the Si-rich films, a completely different behaviour appears, without any optimum annealing temperature. The C – V results show that the D_{it} distribution narrows up to 500 °C (figure 3) but the minimum of D_{it} is almost unchanged (figures 3–5). The SPV indicates almost no difference up to 500 °C and deterioration above that temperature (figures 7 and 8). There is almost complete agreement between both techniques in the range of temperatures in which the data points superimpose (figure 8).

This marked difference between the Si-rich composition and the other two types of films has also been found to occur in other properties. A previous study of the optical absorption in $\text{SiN}_x\text{:H}$ revealed the existence of thermal relaxation processes that were absent in Si-rich films [16]. The same occurred with the defect structure of $\text{SiN}_x\text{:H}$ films and its evolution with annealing temperature [18], which has been shown in figure 5 to have an striking parallelism with the trends of the minimum of D_{it} for the three compositions. In that figure, a significant reduction of N_{db} is observed. This reduction, of more than one order of magnitude, occurs in coincidence with the minimum of D_{it} in the N-rich films, and within reasonable agreement for the near-stoichiometric.

In the Si-rich films, in contrast, the minimum of N_{db} as a function of annealing temperature is barely significant. That means that the relaxation process that causes the decrease of the N_{db} for the other two compositions is not acting so well for the Si-rich samples. The reason behind the differing behaviour of the Si-rich films compared with the N-rich and near-stoichiometric compositions originates from the strain caused by the percolation of Si–Si bond chains through the $\text{SiN}_x\text{:H}$ lattice. It is well known that a percolation threshold exists in $\text{SiN}_x\text{:H}$ at about $x = 1.1$. Below this limit, the

sample is so rich in silicon that chains of Si–Si bonds expand with continuity throughout the network. Because of the high coordination number of Si, the percolation of Si–Si bonds causes a high stress in the $\text{SiN}_x\text{:H}$ film and impedes the relaxation phenomena that take place in the other films. In our case, the Si-rich films have an as-grown composition of $x = 0.97$ and consequently are below the percolation threshold, while the near-stoichiometric have $x = 1.43$ and the N-rich $x = 1.55$. Therefore, the rigidity caused by the tetra-coordinated silicon atoms explains the absence of relaxation processes at moderate temperatures for the Si-rich samples.

A second set of results comes from the trends observed for the flat band potential (V_{FB}) in figures 1 and 2 and the flat band hysteresis in figure 6. Both parameters have decreasing trends with increasing annealing temperatures for the three compositions. This suggests an analogous origin for the density of effective charge in the dielectric (directly related to the value of V_{FB}) and the slow traps located near the interface (responsible for the hysteresis of the high-frequency capacitance curve). Additionally, this charge tends to disappear at the highest RTA temperatures (completely in the N-rich and near-stoichiometric cases and only partially in the Si-rich). In contrast, both D_{it} and N_{db} increase at the highest temperatures (figures 5 and 8). Our previous studies of composition and bonding in films with the same characteristics as those analysed here indicated that dehydrogenation processes took place above a certain threshold temperature. This temperature is approximately coincident to the one that marks the inversion of the trends of D_{it} and N_{db} in the near-stoichiometric samples, and a bit higher in the N-rich case. For the Si-rich composition, it coincides with the increase of the defect density shown in figures 5 and 8. We therefore interpret that the effusion of hydrogen is the cause that puts an end to the thermal relaxation processes and causes damage to the interface and the bulk dielectric. Nevertheless, the density of charge, responsible for the flat band shift and hysteresis, is not affected and it decreases monotonically as the temperature is increased.

4.2. Thick samples

The interesting point of discussion regarding the results of the two thick series (figures 9 and 10) is the different behaviour shown by the annealed near-stoichiometric films in contrast to all the other samples. As it was shown when the results of figure 10 were introduced, the bias voltage sweep is insufficient to bring the device into inversion. Furthermore, a small feature appears in the photovoltage curves for the 500 and 600 °C annealing temperatures. This structure turns into a pronounced flattening in the 900 and 1050 °C treated samples. In the D_{it} spectra (figure 10, right graph) these features appear as peaks, whose position shifts to lower energy levels with increasing annealing temperature, as if they come from the conduction band and move towards the midgap. This is the only case in which we have observed this kind of behaviour in the modulation of the Fermi level. In all the samples of small thickness the D_{it} distributions had U-shaped forms without any remarkable features (figures 3 and 7) and the same occurred for the thick N-rich series (figure 9).

The nature of these peaks in the D_{it} spectra is difficult to interpret. The structure or feature in the V_{ph} – V_{bias} curves is

observed in good agreement in both measuring directions (accumulation to inversion and vice versa) so a non-equilibrium phenomenon is highly improbable. In a first approach, a possible interpretation could be done in terms of a group of states superimposed on the usual distribution of dangling bond states. In such a case, the energy level of those states would shift from next to the conduction band deeper into the gap with increasing annealing temperature. Simultaneously with this shift, the size of the peak becomes more pronounced if we take into account the level of the background distribution, indicating an increased fractional density of the associated states. Nevertheless, the sharp shape of the peaks is unusual for real defect states, and the shift of the energetic level makes it difficult to relate them to a certain structural defect. Instead, a more plausible interpretation is in terms of increasing fluctuations of the surface potential. We can imagine it by adding up different $V_{ph}-V_{bias}$ curves that are shifted along the V_{bias} axis, denoting different parts of the surface area with different values of the surface potential. If there are two preferred values of the surface potential a flat part in the total $V_{ph}-V_{bias}$ curve can arise, leading in the usual evaluation procedure to a peak in the D_{it} distribution. Then, in this case the peaks would not be associated with a real structural defect, but rather to an effect of the evaluation of the data. The sharp shape of the peaks and the shift of their energy levels are in support of this interpretation. One probable origin could be the existence of clusters of different composition at the interface.

5. Conclusions

The effects of RTA processes on the electrical properties of $\text{SiN}_x\text{:H/Si}$ interfaces have been studied by two different methods: $C-V$ and SPV measurements. Three different compositions of the $\text{SiN}_x\text{:H}$ were studied, and it was found that the silicon content plays an essential role in determining the response of the interface to the thermal treatments. For a composition below the percolation threshold of the Si-Si bonds the strain caused by the high coordination number of Si is found to propagate to the interface and prevent any relaxation or interface reconstruction. For compositions above the percolation threshold, the lattice and the interface seem to be much more flexible and the thermal treatments at moderate temperatures cause a significant reduction of D_{it} . In addition, their distribution in the gap becomes wider and more symmetric. The agreement between the results obtained by SPV and $C-V$ methods was found to be excellent. The only significant discrepancy appeared at the temperature that marks the inversion of the trend for the near-stoichiometric films, but was attributed to differences in the samples analysed by each technique.

Not only the influence of the composition of the $\text{SiN}_x\text{:H}$ films was analysed, but also the thickness of the dielectric layer. $\text{SiN}_x\text{:H}$ is characterized by higher stress than other dielectrics commonly used for gate applications, such as SiO_2 , due to a higher average coordination number. When increasing the thickness the negative effects of the stress become much more pronounced. For this reason, two series of thick samples were analysed by SPV (no quasi-static capacitance can be measured in these samples due to the high leakage currents). In the N-rich case, the benefits of the thermal treatments at moderate

temperatures were found to be analogous to the thin samples. In the near-stoichiometric composition, modulation towards inversion is limited by the bias voltage available in our setup. In this case, the thermal treatments produced the appearance of a peak in the D_{it} distribution whose more probable origin is related to fluctuations of the surface potential caused by clusters of different composition at the interface.

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References

- [1] *The SIA Roadmap for Semiconductor Technology* 1997 (Santa Clara, CA)
- [2] Yang H Y, Niimi H and Lucovsky G 1998 *J. Appl. Phys.* **83** 2327
- [3] Niimi H and Lucovsky G 1999 *J. Vac. Sci. Technol. B* **17** 2610
- [4] Wu Y, Lee Y M and Lucovsky G 2000 *IEEE Electron Device Lett.* **21** 116
- [5] Ma Y, Yasuda T and Lucovsky G 1994 *Appl. Phys. Lett.* **64** 2226
- [6] García S, Mártel I, González-Díaz G, Castán E, Dueñas S and Fernández M 1998 *J. Appl. Phys.* **83** 332
- [7] Hugon M C, Delmotte F, Agius B and Courant J L 1997 *J. Vac. Sci. Technol. A* **15** 3143
- [8] Mohammad S N, Tao M, Park D G, Botchkarev A E, Li D and Morkoc H 1996 *Phil. Mag. B* **73** 817
- [9] Park D G, Reed J C and Morkoc H 1997 *Appl. Phys. Lett.* **71** 1210
- [10] Landheer D, Rajesh K, Masson D, Hulse J E, Sproule G I and Quance T 1998 *J. Vac. Sci. Technol. A* **16** 2931
- [11] Lu Z, He S S, Ma Y and Lucovsky G 1995 *J. Non-Cryst. Solids* **187** 340
- [12] Lu Z, Santos-Filho P, Stevens G, Williams M J and Lucovsky G 1995 *J. Vac. Sci. Technol. A* **13** 607
- [13] Park D G *et al* 1996 *J. Vac. Sci. Technol. B* **14** 2674
- [14] Martínez F L, del Prado A, Bravo D, López F, Mártel I and González-Díaz G 1999 *J. Vac. Sci. Technol. A* **17** 1280
- [15] Martínez F L, Mártel I, González-Díaz G, Selle B and Sieber I 1998 *J. Non-Cryst. Solids* **227-230** 523
- [16] Martínez F L, del Prado A, Mártel I, González-Díaz G, Selle B and Sieber I 1999 *J. Appl. Phys.* **86** 2055
- [17] Bohne W, Fuhs W, Röhrich J, Selle B, González-Díaz G, Mártel I, Martínez F L and del Prado A 2000 *Surf. Interface Anal.* **30** 534
- [18] Martínez F L, del Prado A, Mártel I, Bravo D and López F J 2000 *J. Appl. Phys.* **88** 2149
- [19] Heilig K, Flietner H and Reineke J 1979 *J. Phys. D: Appl. Phys.* **12** 927
- [20] Shimizu H and Munakata C 1994 *Appl. Phys. Lett.* **64** 3598
- [21] Kamieniecki E 1985 *J. Appl. Phys.* **57** 2840
- [22] Marsi M *et al* 2000 *Phys. Rev. B* **61** R5070
- [23] Heilig K, Kolbig E and Reineke J 1989 *Phys. Status Solidi a* **114** 579
- [24] Burstein L, Bregman J and Shapira Y 1991 *J. Appl. Phys.* **69** 2312
- [25] Yan Y 1997 *Appl. Phys. Lett.* **71** 407
- [26] García S, Martín J M, Fernández M, Mártel I and González-Díaz G 1996 *Phil. Mag. B* **73** 487
- [27] Lam Y W 1971 *J. Phys. D: Appl. Phys.* **4** 1370
- [28] Nicollian E H and Brews J R 1982 *MOS (Metal Oxide Semiconductor) Physics and Technology* (New York: Wiley)