C–V, DLTS and conductance transient characterization of SiN_x : H/InP interface improved by N₂ remote plasma cleaning of the InP surface

H. CASTÁN, S. DUEÑAS, J. BARBOLLA

Dept. Electricidad y Electrónica, E.T.S.I. Telecomunicación, Campus “Miguel Delibes”, Universidad de Valladolid, 47011 Valladolid, Spain

E. REDONDO, I. MÁRTIL, G. GONZÁLEZ-DÍAZ

Dept. Física Aplicada III (Electricidad y Electrónica), Fac. CC Físicas, Universidad Complutense, 28040 Madrid, Spain

E-mail: helenae@ele.uva.es

Electrical characterization of Al/SiN_x : H/InP structures shows that ECR nitrogen plasma cleaning of InP surfaces gives rise to a noticeable improvement in the interface quality, whereas insulator and semiconductor bulk properties are maintained at a level sufficient to be used as the gate dielectric in MIS devices. Nitrogen plasma exposure was carried out just before the SiN_x plasma deposition without vacuum breaking. To obtain interface state density and to detect deep levels in the semiconductor bulk, deep level transient spectroscopy (DLTS) measurements were carried out. We have also evaluated the insulator damage density, the so-called disorder-induced gap states (DIGS), by means of conductance transient analysis. Our results show that the plasma exposure in N₂ atmospheres is a valuable and simple surface conditioning method.

© 2001 Kluwer Academic Publishers

1. Introduction

The fabrication of III-V material metal-insulator-semiconductor structures to be used in field-effect transistors presents some problems related to insulator-semiconductor interface quality. In this sense, it is crucial to use a dielectric growth technique that minimizes damage effects on the semiconductor surface, such as electron-cyclotron-resonance plasma enhanced chemical-vapor-deposition (ECR-CVD) [1]. In previous studies we have demonstrated that this is a suitable method to obtain excellent SiN_x : H-InP and SiN_x : H-In_{0.53}Ga_{0.47} interfaces. We have also reported on the use of rapid thermal annealing (RTA) treatments to improve interface quality [2, 3] and we have characterized the RTA temperature and dielectric composition influences on the electrical characteristics of ECR-deposited silicon nitride SiN_x : H-InP and SiN_x : H-InGaAs interfaces by capacitance–voltage (C–V), deep-level-transient-spectroscopy (DLTS) and conductance transient (G–t) techniques [4]. In all of these cases, the semiconductor wafer surfaces were not submitted to any treatment prior to the insulator deposition.

In this work we show that a previous cleaning of the InP surface gives rise to a noticeable improvement in the interface quality of the MIS structures. We use ECR nitrogen plasmas to carry out the cleaning of the InP surfaces. Electrical performance of Al/SiN_x : H/InP structures has been analyzed to determine the effect of

the plasma cleaning. The SiN_x : H insulator layers are deposited at 200 °C by using ECR-CVD.

2. Experimental

2.1. Sample description

The InP substrates used in this study are (100) oriented undoped wafers with a carrier concentration of $5 \times 10^{15} \text{ cm}^{-3}$. Samples were degreased with organic solvents; afterwards, they were wet-etched in a conventional chemical bath of HIO₃ : H₂O (10% at weight) for 1 min, and just before being transferred to the vacuum deposition chamber, they were etched in HF:H₂O (1:10) for 15 s in a N₂-filled glove chamber. Nitrogen plasma cleaning was carried out just before 40 nm-thick insulator plasma deposition. Cleaning time duration (15–75 s), microwave power (50–120 W) and N₂ gas pressure (0.07–0.3 Pa) were the variables used to optimize the cleaning step. Once the cleaning process was finished, the insulator deposition was carried out. N₂ and pure SiH₄ were the gases used. The gas fluxes were varied to obtain an insulator composition of $x = 1.55$ ($x = \text{N/Si}$) which, according to a previous study, has been reported to exhibit the lowest interface trap densities [5]. The substrate temperature during the plasma cleaning and deposition process was kept constant at 200 °C. In some samples, RTA (in Ar atmosphere at 500 °C for 30 s) has also been performed to observe the influence of the

thermal process. Afterwards, the top contact (Al) and later, the back contact (AuGe/Au) were evaporated and alloyed for 20 min at 300 °C in an Ar atmosphere. The area of the finished devices was $1.2 \times 10^{-3} \text{ cm}^2$.

2.2. Electrical characterization

The electrical characterization was carried out by using C - V , DLTS and G - t techniques. Both room temperature and 78 K C - V curves exhibit hysteresis phenomena, thus indicating that the interface state distribution follows the well-known disorder-induced gap-state (DIGS) [6] model. According to this model, interface states are distributed both in energy and in space. The spatial extension of the disordered semiconductor region is very narrow, typically several monolayers.

DLTS measurements between 78 and 300 K allow us to obtain the interface trap distribution within the forbidden gap if the bias voltage is chosen so that the MIS capacitor is just at the limit between depletion and weak inversion, and a pulse high enough to drive the capacitors into accumulation is applied in order to fill all interface traps. The D_{it} distribution was deduced from DLTS measurements by means of the expressions [7]:

$$D_u = \frac{\varepsilon_s N_D C_1 [C(t_2) - C(t_1)]}{KT} \frac{1}{[C(t_1)]^3} \frac{1}{\ln(t_2/t_1)} \quad (1)$$

$$E = E_C - KT \ln \left[\sigma_n(E) v_{th} N_C \frac{t_2 - t_1}{\ln(t_2 - t_1)} \right] \quad (2)$$

where $C(t)$ is the capacitance evaluated at time t , C_1 is the capacitance of the insulator, σ_n is the interface states capture cross-section, v_{th} is the thermal velocity of electrons, and N_C is the effective density of states of the conduction band. An energy-independent capture cross-section value of $\sigma_n = 1 \times 10^{14} \text{ cm}^2$ was used in the calculation, which is typically found in InP MIS structures [8].

On the other hand, we can also use DLTS to detect the deep levels present in the semiconductor bulk. In this case, the height of the pulse and the bias voltage are chosen so that the sample remains in strong inversion and therefore interface states remain empty, so capacitance transients correspond to changes in the occupation factor of the deep levels occurring when bias pulses are applied.

Finally, G - t measurements provide quantitative information about the disordered induced damage states. As has been published elsewhere [4, 9], from the experimental conductance transients, $G(t)$, we can obtain the DIGS state density (N_{DIGS}) as a function of the spatial distance to the interface (x_c) and of the energy position $E' - E(x_c, t)$, where E' stands for the conduction band edge of the insulator, as follows:

$$N_{DIGS} = \frac{\Delta G / \omega}{0.4 q A} \quad (3)$$

$$x_c(t) = x_{on} \ln(\sigma_o v_{th} n_s t) \quad (4)$$

$$E' - E(x_c, t) = H_{eff} + kT \ln \left(\frac{\sigma_o v_{th} N_C}{\omega / 1.98} \right) - kT \frac{x_c(t)}{x_{on}} \quad (5)$$

where $x_{on} = \hbar / (2\sqrt{2m_{eff}H_{eff}})$ is the tunneling decay length, σ_o is the carrier capture cross-section value for

$x=0$, v_{th} is the carrier thermal velocity in the semiconductor, and n_s is the free carrier density at the interface. Finally, H_{eff} is the insulator-semiconductor energy barrier for minority carriers.

3. Results and discussions

Fig. 1 shows the interface trap distribution within the forbidden gap obtained by DLTS for the unexposed and plasma-exposed devices, as a function of exposure time (a), microwave power (b) and N_2 pressure (c). The lower values of the trap density for the plasma-exposed devices are quite apparent. This interface improvement is probably due to the fact that the main effect of the N_2 plasma exposure is an electrical passivation of the InP

Figure 1 Interface state density measured by DLTS for unexposed and plasma-exposed devices, as a function of (a) exposure time, (b) microwave power, (c) N_2 pressure.

surface, probably due to the formation of P–N and/or In–P–N complexes. The presence of these complexes on InP [10] and GaP [11] has been described. According to Fig. 1a intermediate values of exposure time (30, 45 s) are better than extreme ones (15, 60 and 75 s). Regarding the microwave power, we can see in Fig. 1b the presence of a minimum in the trap density corresponding to 60 W. On the other hand, the N₂ plasma pressure does not seem to have a relevant influence, except for the fact that 0.3 Pa is the worst value (Fig. 1c). As has been reported elsewhere [12], we can conclude that to obtain an interface of good quality the optimum conditions of N₂ plasma cleaning are the following: 30 s for plasma exposure time, 60 W for microwave power and 0.07 Pa for the N₂ pressure. Longer exposure time and higher microwave power or N₂ gas pressure induce large damage at the SiN_x : H/InP interface. This could probably be due to a high ion density and/or ion energy bombardment that degrades the interface and leads to a strong P loss at the surface.

Fig. 2 shows the DIGS damage obtained from room temperature–100 kHz G - t measurements for the unexposed and plasma-exposed devices, as a function of exposure time (a), microwave power (b) and N₂ gas pressure (c). We can see that DIGS damage exhibits a behavior opposite to interface traps, i.e., DIGS damage increases with the plasma cleaning. This fact can be explained in terms of nitrogen atoms deposited during the cleaning that moves into the insulator when it is grown. However, under optimum conditions plasma-exposed devices have insulator characteristics ($\rho = 1.2 \times 10^{15} \Omega \text{ cm}$), $E_B = 3.5 \text{ MV cm}^{-1}$ good enough to be used as the gate dielectric in MIS devices.

Fig. 3 shows the interface trap distribution within the forbidden gap (a) and the DIGS damage (b) corresponding to: unexposed substrate (u-ex), N₂ plasma-exposed substrate at the optimum conditions (pl-ex), rapid thermal annealed structure (RTA), and N₂ plasma-exposed substrate at the optimum conditions and rapid thermal annealed structure (pl-ex + RTA). This time we can also observe an inverse correlation between interface traps and DIGS damage. Regarding the DLTS results, we conclude that the plasma-exposed device is the best of the four processed devices. Both RTA and plasma cleaning separately improve interface characteristics, but RTA treatments do not improve the interface quality of plasma-exposed devices. This could be due to rapid thermal annealing breaking P-type bonds formed during the N₂ plasma exposure step. Indeed, in previous studies [2, 13], we have observed that RTA improves the interface quality for temperatures below 600 °C, but it degrades at higher temperatures, having optimum values for temperatures in the range 400–500 °C. This can be explained in terms of two competing mechanisms: First, RTA promotes nitrogen atoms from the insulator to the interface repairing defects related to phosphorous vacancies (V_P). Simultaneously, the thermal annealing breaks In–P bonds at the interface creating new phosphorous vacancies. At temperatures below 600 °C the first mechanism seems to be dominant and then the density of V_P -like defects decreases. However, at temperatures higher than 600 °C the second mechanism becomes dominant and an effective degradation of the interface occurs.

Figure 2 DIGS damage obtained from room temperature–100 kHz G - t measurements for unexposed and plasma-exposed devices, as a function of (a) exposure time, (b) microwave power, (c) N₂ pressure.

When nitrogen plasma cleaning is applied previously to the SiN_x : H film deposition, nitrogen plasma atoms recover all the V_P defects at the semiconductor interface. Therefore, when RTA is applied only the second mechanism takes place and the interface state density increases at all annealing temperatures.

Moreover, by using the DLTS technique, we have also studied the deep levels existing in the InP bulk. An electron trap, whose corresponding emission energy is 0.45 eV below the minimum of the conduction band, has been found in all the samples. As we have explained

Figure 3 Experimental results obtained to unexposed substrate (u-ex), N_2 plasma-exposed substrate at the optimum conditions (pl-ex), rapid thermal annealed structure (RTA) and N_2 plasma-exposed substrate at the optimum conditions and rapid thermal annealed structure (pl-ex + RTA): (a) interface state density measured by DLTS, (b) DIGS damage obtained from room temperature–100 kHz G - t measurements.

elsewhere [13], this level could be related to phosphorus vacancies (V_P) or complexes involving V_P . We have studied the deep level density values as a function of the cleaning plasma parameters, and we have concluded that the sample submitted to the cleaning plasma at the optimum conditions shows the lowest deep level density. Fig. 4 shows DLTS spectra corresponding to an emission time constant of 23.7 ms, for the unexposed and plasma-exposed devices, as a function of exposure time (a), microwave power (b) and N_2 gas pressure. From this, we clearly conclude that the optimum conditions of nitrogen plasma cleaning are the above-mentioned: 30 s for plasma exposure time, 60 W for microwave power and 0.07 Pa for the N_2 pressure. The shift observed in the deep level peak is merely an artefact. As is well known, the formation of the inversion layer gives rise to a dummy peak in DLTS curves at high temperatures that produces distortions on the true spectra of deep levels. This effect is more apparent the lower the deep-level density.

4. Conclusions

By using C - V , DLTS and G - t techniques, we have carried out a parametric study of the influence of ECR nitrogen plasma exposure on the electrical characteristics of $Al/SiN_x : H/InP$ structures. DLTS results show that

Figure 4 DLTS spectra corresponding to an emission time constant of 23.7 ms for unexposed and plasma-exposed devices, as a function of (a) exposure time, (b) microwave power, (c) N_2 pressure.

plasma cleaning improves interface quality and deep-level density in the semiconductor bulk, and that the optimum conditions of nitrogen plasma cleaning are the following: 30 s for plasma exposure time, 60 W for microwave power and 0.07 Pa for the N_2 pressure. On the other hand, G - t measurements indicate that DIGS damage increases when plasma cleaning is performed.

However, plasma-exposed devices have overall insulator characteristics suitable for use as the gate dielectric in MIS devices. The main effect of the nitrogen plasma exposure is an electrical passivation of the InP surface, probably due to the formation of P–N and/or In–P–N complexes. When the insulator is grown, nitrogen atoms can move into it, thus increasing DIGS damage. A post-deposition RTA treatment does not improve the interface quality because RTA breaks P-type bonds formed during the N₂ plasma exposure step.

Acknowledgments

The authors would like to thank C.A.I. de Implantación Iónica from the Complutense University in Madrid for technical assistance with the ECR-CVD system. This research was partially supported by the Spanish DGESIC under Grants No. TIC 1FD97-2085 and TIC 98/0740.

References

1. A. KAPILA, X. SI and V. MALHORA, *Appl. Phys. Lett.* **62** (1993) 2259.
2. E. REDONDO, N. BLANCO, I. MÁRTIL, G. GONZÁLEZ-DÍAZ, R. PELÁEZ, S. DUEÑAS and H. CASTÁN, *J. Vac. Sci. Technol. A* **17** (1999) 2178.
3. E. REDONDO, N. BLANCO, I. MÁRTIL and G. GONZÁLEZ-DÍAZ, *Appl. Phys. Lett.* **74** (1999) 991.
4. H. CASTÁN, S. DUEÑAS, J. BARBOLLA, E. REDONDO, N. BLANCO, I. MÁRTIL and G. GONZÁLEZ-DÍAZ, *Microelectron Reliab* **40** (2000) 845.
5. S. GARCÍA, I. MÁRTIL, G. GONZÁLEZ-DÍAZ and M. FERNÁNDEZ, *Semicond. Sci. Technol.* **12** (1997) 1650.
6. L. HE, H. HASEGAWA, T. SAWADA and H. OHNO, *J. Appl. Phys.* **63** (1988) 2120.
7. E. H. NICOLLIAN and J. R. BREWS, "MOS Physics and Technology", (Wiley, New York, 1982).
8. T. HASHIZUME, H. HASEGAWA, R. RIEMENSCHNEIDER and H. L. HARTNAGEL, *Jpn. J. Appl. Phys.* **33** (1994) 727.
9. S. DUEÑAS, R. PELÁEZ, H. CASTÁN, R. PINACHO, L. QUINTANILLA, J. BARBOLLA, I. MÁRTIL and G. GONZÁLEZ-DÍAZ, *Appl. Phys. Lett.* **71** (1997) 826.
10. M. LOSURDO, P. CAPEZZUTO, G. BRUNO, G. LEO and E. A. IRENE, *J. Vac. Sci. Technol. A* **17** (1999) 2194.
11. T. HASHIZUME, *Appl. Phys. Lett.* **75** (1999) 615.
12. E. REDONDO, I. MÁRTIL, G. GONZÁLEZ-DÍAZ, H. CASTÁN and S. DUEÑAS, submitted to *J. Vac. Sci. Technol.*
13. R. PELÁEZ, H. CASTÁN, S. DUEÑAS, J. BARBOLLA, E. REDONDO, I. MÁRTIL and G. GONZÁLEZ-DÍAZ, *J. Appl. Phys.* **86** (1999) 6924.

*Received 23 October 2000
and accepted 12 February 2001*