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Comparison between n-type and p-type Al/SiN_x:H/In_{0.53}Ga_{0.47}As devices deposited by electron cyclotron resonance technique

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Abstract. The influence of the semiconductor doping type over the electrical properties of Al/SiN_x:H/In_{0.53}Ga_{0.47}As metal–insulator–semiconductor (MIS) devices has been studied using capacitance–voltage ($C-V$) and current–voltage ($I-V$) measurements. The $C-V$ data show that the SiN_x:H/p-In_{0.53}Ga_{0.47}As interface is more defective than the SiN_x:H/n-In_{0.53}Ga_{0.47}As one. In both n- and p-type MIS structures, the interface trap density (D_{it}), the electrical breakdown field (E_B) and the resistivity (ρ) are highly dependent on the insulator composition. On the other hand, rapid thermal annealing treatments at temperatures up to 600 °C induce a gradual improvement of both interface and SiN_x:H bulk quality on n-type MIS devices, whereas a continuous degradation of the SiN_x:H/p-In_{0.53}Ga_{0.47}As interface properties is observed. Zinc out-diffusion from p-In_{0.53}Ga_{0.47}As towards the insulator–semiconductor interface could explain the poorest electrical characteristics of the MIS structures based on a p-type semiconductor.

1. Introduction

In_{0.53}Ga_{0.47}As is a very attractive semiconductor material for field effect device applications. In fact, the excellent electron transport properties of this III–V ternary compound make it very interesting for high-speed devices, such as metal–insulator–semiconductor field effect transistors (MISFETs). However, it is well known that there are drain current drift instabilities in In_{0.53}Ga_{0.47}As MISFETs [1], which Mui *et al* associated with tunnelling-related trapping in the insulator and at the interface [2, 3]. So, good control of the insulator–semiconductor interface and the insulator quality is required in order to improve the fabrication process of devices based on metal–insulator–semiconductor (MIS) structures. Recently, post-deposition rapid thermal annealing (RTA) treatments have been shown to improve the interface properties of the Al/SiN_x:H/In_{0.53}Ga_{0.47}As MIS diodes [4, 5]. On the other hand, it has been proved that the deposition of the so-called Si interface control layer (ICL) on the semiconductor surface, yields MIS capacitors on III–V compounds with very low midgap trap densities [5–7]. However, the ICL does not produce successful MISFET operation, probably due to the fact that band offsets between the Si layer and the semiconductor lead to a two-dimensional electron gas in the Si, which prevents inversion in the III–V semiconductor,

as Chen *et al* explained in GaAs-based FET devices [8]. One of the aims of this work is to show that high-quality SiN_x:H/In_{0.53}Ga_{0.47}As interfaces could be obtained without using an additional Si interlayer.

There are several investigations in the literature concerning MIS devices deposited on n-In_{0.53}Ga_{0.47}As [5, 9–11], but little work has been done with regard to the characterization of SiN_x:H/In_{0.53}Ga_{0.47}As structures fabricated with p-type substrates.

In this paper, we present a comparative study of the electrical properties of SiN_x:H/In_{0.53}Ga_{0.47}As structures made over the p- and n-type semiconductors. The effectiveness of the low-temperature electron cyclotron resonance (ECR) plasma technique, used for the dielectric deposition, will be proved by the quality of the results obtained from the capacitance–voltage ($C-V$) and current–voltage ($I-V$) measurements carried out in the Al/SiN_x:H/In_{0.53}Ga_{0.47}As devices. The different behaviour of the electrical properties of n- and p-type MIS structures with post-deposition RTA treatments will also be discussed.

2. Experimental

The commercial In_{0.53}Ga_{0.47}As epilayers (supplied by Epitaxial Products International Ltd, Cypress Drive, St Mellons, Cardiff, UK, CF3 OEG) used in this study were

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grown by metal organic vapour phase epitaxy on (100) InP. Two different kinds of ternary semiconductor have been used: n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (S doped), with a net donor concentration of $6.6 \times 10^{15} \text{ cm}^{-3}$, and p- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (Zn doped), with a net acceptor concentration of $1.1 \times 10^{16} \text{ cm}^{-3}$. The semiconductor surface was ultrasonically degreased with organic solvents, and treated in $\text{HCl}:\text{H}_2\text{O}$ (1 : 3) just before being transferred to the vacuum deposition chamber. Obviously, an *in situ* characterization of the semiconductor surface (by means of scanning tunnelling microscopy or other related techniques) just prior to the gate dielectric deposition would be very useful. However, our deposition chamber does not allow such characterization, so we do not know the oxidized status of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface.

$\text{SiN}_x:\text{H}$ films, 500 Å thick, were deposited by the ECR plasma technique, with N_2 and pure SiH_4 as precursor gases. The gas flux ratio, $R = [\text{N}_2]/[\text{SiH}_4]$, was varied from 1 to 9 to obtain different insulator compositions: from Si-rich samples ($R < 1.6$) to N-rich ones ($R > 1.6$) [12]. Microwave power (100 W), substrate temperature (200 °C), and total pressure (0.6 mTorr) were kept constant in all the experiments. The top contacts were obtained by a thermally evaporated array of Al dots, whereas we used AuGe/Au or AuZn/Au metallizations to form the back ohmic electrode over n- and p-type wafers, respectively. Finally, the contacts were alloyed simultaneously at 300 °C over a period of 20 min, in Ar atmosphere. Typical device areas were $1.12 \times 10^{-3} \text{ cm}^2$.

Some samples were exposed to different RTA processes. The annealing time was kept constant at 30 s, with the RTA temperature varying from 400 to 700 °C.

MIS structures were characterized with C - V —both quasi-static (C_q) and high-frequency (C_h) curves—and I - V measurements performed in accumulation. Both sets of data were obtained with a Keithley model 82 system. From the C - V data, the interface trap density (D_{it}) distribution has been calculated using the high-low-frequency capacitance method [13]. From the I - V curves, the resistivity (ρ) and the breakdown field (E_B) have been obtained. The value of E_B was equal to the field at which the MIS current reaches $1 \mu\text{A cm}^{-2}$ [14], whereas the ρ data were obtained from the slope of the I - V curve at low fields. The D_{it} , ρ and E_B were obtained by averaging the measurements of three different electrodes of each sample. As we will see in the discussion, to evaluate more precisely E_B for the dielectric deposited on n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates, it was necessary to make $\text{SiN}_x:\text{H}/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MIS structures with thinner $\text{SiN}_x:\text{H}$ films. To this end, the E_B determination was performed on capacitors with ≈ 200 Å-thick $\text{SiN}_x:\text{H}$ films.

It should be pointed out that the different dielectric compositions used on MIS diodes may be the cause of the presence of charge centroids or current leakage mechanisms in the dielectric that may influence the reported values for ρ . Since we have not analysed such possibilities, the results we will present on the resistivity values should be analysed in terms of trends that this parameter exhibits, rather than as an exact value of it.

Figure 1. High-frequency and quasi-static C - V curves versus gate voltage for $\text{Al}/\text{SiN}_x:\text{H}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors: (a) p-type semiconductor; (b) n-type semiconductor. The $\text{SiN}_x:\text{H}$ films were deposited with a gas flux ratio of $R = 5$.

3. Results and discussion

3.1. Characterization of non-annealed MIS devices

Figures 1(a) and (b) present the quasi-static and high-frequency C - V curves of p- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{SiN}_x:\text{H}$ and n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{SiN}_x:\text{H}$ interfaces, respectively, where the insulator film was deposited with a gas flux ratio of $R = 5$. The main differences between the curves are in relation to the hysteresis values and the frequency dispersion in the accumulation zone: the hysteresis varies from 900 meV (in the p-type MIS structure), to 240 meV (in the n-type one), whereas the frequency dispersion is about 8% and 3%, respectively. It is worth noting that these dispersion values are calculated as the difference between the C_q and C_h curves in the accumulation regime. If we use a less limiting criteria (for instance, the difference between 1 kHz and 1 MHz C - V curves), the dispersion measured on n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MIS capacitors would be near zero, as Wang *et al* reported [15]. From the above data, it is clear that MIS devices deposited on an n-doped semiconductor show minor bulk insulator charge and lower interface trap density than those obtained on p-type ones. Also, the slope of the high-frequency curve from accumulation to strong inversion is lower for the p- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{SiN}_x:\text{H}$ interface, denoting the presence of a significant density of interface traps near the band edges in the p-type MIS device.

Figure 2 displays the distributions of the D_{it} obtained from the C - V curves of figure 1, for both p- and n-type $\text{SiN}_x:\text{H}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfaces. Both distributions scan about 0.4 eV of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap (0.75 eV). However, this fact is not indicative of the high interface trap density in the other half of the bandgap, because we must bear in mind that the high-low-frequency method is essentially valid in the depletion regime [13]. So, if we analyse both n- and p-type MIS structures, with similarly doped InGaAs substrates, and assuming that the insulator-semiconductor interface has the same defects structure, we could characterize a greater region of the semiconductor bandgap. This fact occurs because the gate bias at which the MIS device is under depletion condition is different in $\text{SiN}_x:\text{H}/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ or $\text{SiN}_x:\text{H}/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfaces. Therefore, we can consider that

Figure 2. Distribution of interface trap density versus gap energy relative to the midgap, for MIS devices on p-In_{0.53}Ga_{0.47}As (■) and n-In_{0.53}Ga_{0.47}As (△). SiN_x:H films were deposited with a flux gas ratio of $R = 5$.

the trap distribution of a SiN_x:H/In_{0.53}Ga_{0.47}As interface could be the composition of both D_{it} distributions plotted in figure 2. From this figure, we can also deduce the pile-up of the interface trap density near the semiconductor valence band because, in p-type MIS devices, the Fermi level could not scan energies close to that band edge.

The values for the minimum of D_{it} shown in figure 2, though higher than those obtained in Si-based MIS devices (that are below 10^{10} eV⁻¹ cm⁻²) [13], are similar to those reported by other authors on n-In_{0.53}Ga_{0.47}As that have demonstrated reasonably good MISFET operation [2, 3, 5]. Notwithstanding this, an evaluation of the operation of such dielectrics on MISFET devices is necessary to unambiguously assess the gate quality of SiN_x:H deposited by the ECR plasma method described here.

Figure 3 shows the minimum of the interface trap density as a function of the gas flux ratio, R , for the different MIS structures investigated. It is clearly seen that the minimum of D_{it} is always better for the devices grown over the n-type semiconductor, whereas the dependence with R is almost the same for both n- and p-type interfaces: higher values of D_{it} minimum are exhibited for dielectric films deposited at $R = 1$ or 1.6 (which are Si-rich films, [12]), being indicative of a defective interface. As the dielectric becomes N-rich ($R \geq 5$), lower values of the minimum of D_{it} are measured. A slightly different behaviour between both types of MIS structures is observed for the highest value of the gas flux ratio ($R = 9$, when the dielectric has the higher N content), which we cannot explain satisfactorily.

In both cases, the minimum values of D_{it} measured (9.4×10^{11} cm⁻² eV⁻¹ for p-type and 6.1×10^{11} cm⁻² eV⁻¹ for n-type MIS structures) are among the lowest data reported for non-annealed *ex situ* SiN_x:H/In_{0.53}Ga_{0.47}As interfaces [3].

In figure 4, we present E_B and ρ as a function of the gas flux ratio, R , measured on both n- and p-type SiN_x:H/In_{0.53}Ga_{0.47}As devices. MIS structures obtained with $R = 9$ showed E_B higher than 4 MV cm⁻¹, but this could not be measured on 500 Å-thick samples because of experimental limitations. On samples with thinner dielectrics (≈ 200 Å), we have measured E_B values of 6 MV cm⁻¹. However, we have not further analysed the

Figure 3. Minimum values of the interface trap density (D_{it}) versus gas flux ratio, R , for MIS devices on p-In_{0.53}Ga_{0.47}As (■) and n-In_{0.53}Ga_{0.47}As (△).

Figure 4. Breakdown field (full symbols) and resistivity (open symbols) versus R , for p-type (■) and n-type (△) SiN_x:H/In_{0.53}Ga_{0.47}As.

interface characteristics of these devices (i.e., we have not obtained the D_{it} distribution), because we have found that the dielectric thickness has a pronounced influence on the insulator/semiconductor characteristics. Details about this fact can be found elsewhere [16].

Figure 4 reveals that both E_B and ρ increases when the gas flux ratio R changes from 1.6 to 9, denoting that both magnitudes improve in both n- and p-type substrates, as the insulator becomes N-rich. This behaviour is usually found in SiN_x:H deposited by plasma techniques, as reported by Tao *et al* [17] and Hugon *et al* [18], and it is directly related to the densities of Si-H and N-H bonds present in the dielectric film [19]. In Si-rich samples (films deposited at $R \leq 1.6$), the concentration of Si-H bonds is high, denoting also a high concentration of Si-Si bonds. These bonds lead to an extremely rigid tetrahedral structure, promoting a high density of silicon-dangling bonds that are electrically active defects. On the other hand, in N-rich films, $R > 1.6$, the N-H bonds are predominant. These bonds are more stable than Si-Si ones, and give a more flexible insulator structure due to the trigonal coordination of the N bonds.

As we can see in figure 4, the improvement of the bulk electrical properties of the SiN_x:H with the gas flux ratio and, as a consequence, when the nitrogen content of the dielectric increases, is more significant for n-type MIS structures. In fact, E_B increase from 1.2 MV cm⁻¹, for nearly

Figure 5. Distributions of interface trap density versus gap energy relative to the midgap for MIS devices on n-In_{0.53}Ga_{0.47}As: non-annealed (Δ), after a RTA cycle at different temperatures, ($\bullet$) 500 °C and ($\square$) 600 °C. SiN_x:H films were deposited with $R = 5$.

stoichiometric films ($R = 1.6$), to more than 4 MV cm^{-1} (8 MV cm^{-1} on the thinnest films), for N-rich films ($R = 9$). On the p-type In_{0.53}Ga_{0.47}As, the electrical properties of the dielectric are less dependent on the gas flux ratio, showing a slight increase of E_B with R , from 1.75 to 2.25 MV cm^{-1} , while ρ remains almost constant at about $10^{16} \Omega \text{ cm}$ for all the values of R analysed. This result was already found by other authors for SiN_x:H films deposited by plasma techniques on III–V semiconductor compounds [18, 20].

From the previous results, we deduced that the bulk electrical properties of the SiN_x:H are dependent on the doping type of the semiconductor substrate [18]. It should be noted that the only difference between the two types of In_{0.53}Ga_{0.47}As epilayers used in this study is the doping element, that is, sulfur and zinc for the n- and p-type epilayers, respectively, as we have already indicated in the experimental section. The influence of the doping type on the electrical properties of the MIS structures analysed in this work will be clarified in the next section.

3.2. Characterization of rapid thermal annealed MIS devices

Figure 5 depicts the D_{it} distribution of a non-annealed SiN_x:H/n-In_{0.53}Ga_{0.47}As structure (with the SiN_x:H deposited at $R = 5$), and also the same distribution for two different MIS devices after RTA cycles at 500 and 600 °C, respectively. The trap distribution becomes wider as the annealing temperature increases up to 600 °C, scanning up to 0.55 eV of the semiconductor bandgap. Moreover, the minimum of D_{it} decreases as the annealing temperature increases.

The D_{it} distribution of a non-annealed SiN_x:H/p-In_{0.53}Ga_{0.47}As structure is shown in figure 6, together with the distributions of another two p-type MIS devices annealed at 500 and 600 °C, respectively. Unlike the behaviour observed in n-doped structures, Al/SiN_x:H/p-In_{0.53}Ga_{0.47}As devices exhibit an evident degradation with the annealing temperature: the minimum of D_{it} increases with RTA temperature, whereas the D_{it} of annealed structures scans across the bandgap about 0.25 eV less than in non-annealed samples.

Figure 6. Distributions of interface trap density versus gap energy relative to the midgap for MIS devices on p-In_{0.53}Ga_{0.47}As: non-annealed (Δ), after a RTA cycle at different temperatures, ($\bullet$) 500 °C and ($\square$) 600 °C. SiN_x:H films were deposited with $R = 5$.

Figure 7. Minimum values of the interface trap density (D_{it}) versus RTA temperature, for MIS devices on p-In_{0.53}Ga_{0.47}As ($\blacksquare$) and n-In_{0.53}Ga_{0.47}As (Δ).

A comparison between the minimum of D_{it} for both n- and p-type SiN_x:H/In_{0.53}Ga_{0.47}As devices, as a function of the RTA temperature, is plotted in figure 7. It is worth noting that there is a continuous decreasing of the minimum of D_{it} as the annealing temperature increases up to 600 °C for n-type MIS devices (7.5×10^{11} – $3.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$), and a sharp increase for higher temperatures. The behaviour shown in p-type devices is quite different, because the minimum of D_{it} increases from 9.5×10^{11} to $7 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ as the temperature increases from 300 to 700 °C.

The minimum of D_{it} obtained for the n-type MIS device annealed at 600 °C ($3.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$) is similar to those obtained in In_{0.53}Ga_{0.47}As [5] or GaAs [15] MIS capacitors, with a Si ICL deposited between the insulator and the III–V semiconductor.

Thus, from the C–V measurements we conclude that an increase of the RTA temperature up to 600 °C produces a gradual improvement in the electrical quality of the interface of n-type SiN_x:H/In_{0.53}Ga_{0.47}As devices. On the other hand, a progressive degradation in the insulator–semiconductor interface is observed when a p-type In_{0.53}Ga_{0.47}As substrate is used.

In relation to the electrical properties of the insulator, figure 8 plots E_B as a function of the RTA temperature.

Figure 8. Breakdown field versus annealing temperature, for p-type (■) and n-type (Δ) Al/SiN_x:H/In_{0.53}Ga_{0.47}As devices. The SiN_x:H films were deposited with $R = 5$.

Figure 9. Resistivity versus annealing temperature, for p-type (■) and n-type (Δ) Al/SiN_x:H/In_{0.53}Ga_{0.47}As devices. The SiN_x:H films were deposited with $R = 5$.

MIS devices made on p-doped substrates exhibited E_B values that increase up to 600 °C, reaching the maximum values of 3.5 MV cm⁻¹. On the other hand, on n-doped MIS diodes, E_B was higher than 4 MV cm⁻¹ on 500 Å-thick SiN_x:H films in the range 400–600 °C of RTA temperature. On the thinnest films, E_B reaches values comprised between 7 and 8 MV cm⁻¹, with a temperature dependence similar to that shown in figure 8. At temperatures higher than 600 °C, E_B decrease significantly.

Concerning the resistivity, a different result was found. Figure 9 shows ρ for n- and p-type MIS devices, as a function of the annealing temperature. Although non-annealed p-type samples exhibit slightly higher values of ρ than n-type ones (6×10^{15} Ω cm compared with 1×10^{15} Ω cm), the RTA treatment promotes a gradual decreasing for this parameter down to 2.2×10^{15} Ω cm for MIS devices deposited on p-In_{0.53}Ga_{0.47}As, whereas on n-type samples, an improvement of ρ up to 8×10^{15} Ω cm is measured.

The general improvement with annealing temperature of both bulk and interface properties of n-type MIS devices has been found by our research group in SiN_x:H/Si [21], and SiN_x:H/n-InP [22] structures, and it has been explained in terms of a thermal relaxation and a reconstruction of the insulator lattice and its interface. This explanation is only tentative, given that many other processes could be responsible for the reported results.

Regarding the influence of substrate doping type, its influence on the SiN_x:H bulk properties is quite evident. In fact, both E_B and ρ are lower for p-type than for n-type annealed structures. Similar results, concerning E_B , were found by Hugon *et al* in Al/SiN_x:H/Si structures [18] deposited by distributed ECR. These authors attributed the lower critical fields obtained in p-type MIS devices, compared to the n-type ones, to the net fixed charge density that depends on MIS structures.

There are no references in the literature in relation to anomalous diffusion of S impurities in In_{0.53}Ga_{0.47}As; however, it is well known that the Zn-diffusion problems exist in III–V semiconductor technology [23–25]. The diffusion of Zn impurities from the semiconductor bulk towards the SiN_x:H/In_{0.53}Ga_{0.47}As interface during the annealing step could conduct to the poorest insulator–semiconductor interfaces, explaining the higher values of interface trap density obtained in p-type MIS devices, compared with the n-type ones. On the other hand, a possible Zn loss through the insulator could explain the degradation of the resistivity with annealing temperature observed in Zn-doped structures. Therefore, we tentatively conclude that the post-deposition RTA treatment does not improve the interface and bulk properties of MIS structures deposited on Zn-doped In_{0.53}Ga_{0.47}As semiconductors. As we have already explained in the previous paragraph, other different possibilities may explain the observed behaviour of ρ ; for instance, the presence of breakdown currents based on filaments, possibly initiated by a spiky structure of the MIS diode.

4. Conclusions

In summary, the electrical properties of both SiN_x:H films (obtained by the ECR technique) and SiN_x:H/In_{0.53}Ga_{0.47}As interfaces have been studied as a function of the insulator composition, post-deposition RTA treatments and doping type of the semiconductor material. The insulator composition plays a significant role on the interface and bulk properties of both SiN_x:H/n-In_{0.53}Ga_{0.47}As and SiN_x:H/p-In_{0.53}Ga_{0.47}As structures, with better values of D_{it} , ρ and E_B on those devices deposited with high values of the gas flux ratio ($R \geq 5$), which yield N-rich insulator films. The bulk properties of the SiN_x:H are clearly dependent on the semiconductor type doping. In general, MIS devices grown on n-type In_{0.53}Ga_{0.47}As present higher electrical performance than p-type ones, even after RTA treatments.

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