PERGAMON

Microelectronics Reliability 40 (2000) 837–840

MICROELECTRONICS RELIABILITY

www.elsevier.com/locate/microrel

N_2 remote plasma cleaning of InP to improve SiN_x:H/InP interface performance

E. Redondo *, M.N. Blanco, I. Mártil, G. González-Díaz

Department of Física Applicada III (Electricidad y Electrónica), Fac. CC. Físicas, Universitat Complutense, Avda. Complutense sln, 28040 Madrid, Spain

Abstract

Cleaning of InP surfaces using electron cyclotron resonance (ECR) nitrogen plasmas has been studied. Electrical performance of Al/SiN_x:H/InP structures has been analysed to determine the effect of the plasma cleaning. The SiN_x:H insulator layers are deposited at 200°C using an ECR chemical vapour deposition technique. It is observed that a 30 s low-power (60 W) ECR N_2 plasma treatment of InP surface reduces the interface defects and improves the resistivity and breakdown field values of the SiN_x:H.

1. Introduction

InP is a well-known material for high frequency and optoelectronic device applications. Much effort has been devoted to the study of the electrical properties of InP metal–insulator–semiconductor field effect transistor (MISFET) devices. However, the main problem of these devices is still that they exhibit instabilities in the long-term operation mode. As well known, the trap states present at the semiconductor surface and at the gate insulator are responsible for the observed drain current drift by capturing some fraction of the induced channel electrons [1]. So it seems to be mandatory to control the insulator/semiconductor interface chemistry and morphology.

Different cleaning processes have been tested and, as a result, the characteristics of the InP surface are strongly affected by the cleaning procedure used. In fact, with the so-called "wet chemical etching", which is an ex situ process, it is not possible to completely remove the carbon and oxygen contaminants [2]; with the "thermal desorption", which requires high temperatures, partial decomposition of the InP substrate is caused [3]; the "Ar ion sputtering" often leads to lattice disruption by ion bombardment [4]; the "in-situ H_2 plasma cleaning" often leads to a preferential etching of the volatile element (P) during the plasma exposure [5]; and the "in-situ O_2 plasma cleaning" removes carbon contaminants at InP surface but leads to an undesirable oxidation of the surface [6].

Because of the reasons described above, we propose the use of N_2 plasma cleaning. Due to this, an atom does not produce heavy ions such as Ar, it can passivate the InP surface. Further, it presents the advantage of being one of the precursor gases in the deposition of SiN_x:H films.

In this article, results on InP in-situ cleaning by N_2 ECR-plasma are presented. The effectiveness in the surface cleaning of the remote N_2 plasma is compared with the conventional wet-etching, and is analysed by the study of the capacitance–voltage and current–voltage curves in Al/SiN_x:H/InP MIS devices.

2. Experimental

The InP substrates used in this study were (1 0 0) oriented undoped wafers with carrier concentration of 5×10^{15} cm^{-3}. Samples were degreased with organic solvents; afterwards, they were wet-etched in a conventional chemical bath of HIO_3:H_2O (10% at weigh) for 1 min, and just before being transferred to the vacuum deposition chamber, they were etched in HF:H_2O (1:10) for 15 s. Nitrogen plasma cleaning was carried out just before the plasma insulator deposition. The cleaning

* Corresponding author. Tel.: +34-91-394-44-35; fax: +34-91-394-51-96.

E-mail address: fannyr@eucmax.sim.ucm.es (E. Redondo).

0026-2714/00/$ - see front matter
PII: S0026-2714(99)00322-4

time duration, microwave power and N_2 gas pressure were the variables analysed to optimise the cleaning step.

Once the cleaning process was finished, the insulator deposition was carried out. N_2 and pure SiH_4 were the gases used. The gas fluxes were ranged to obtain an insulator composition of $x = 1.55$ ($x = N/Si$), which according to previous articles [7] has been reported to exhibit the lowest interface trap densities. The substrate temperature during the plasma cleaning and deposition process was kept constant at 200°C. In some samples, rapid thermal anneals have also been performed to observe the influence of the thermal process.

Then the top contact (Al) and later, the back contact (AuGe/Au) were evaporated on the structure. Finally, these contacts were alloyed for 20 min at 300°C in an Ar atmosphere.

To compare these results with those obtained using other plasma cleanings, we have prepared some samples with an O_2 plasma cleaning before insulator deposition with the same plasma parameters which have been considered optimum in the N_2 plasma cleaning.

MIS structures were characterised measuring the capacitance–voltage (C–V) characteristics – quasi-static (C_q) and high-frequency (C_h) curves – and the current–voltage curves (I–V) with a Keithley Model 82 system. From the C–V measurements, the interface trap density (D_{it}) distribution has been calculated using the high–low frequency method.

From the I–V curves, the resistivity and the breakdown field (at 1 μA/cm^2) have been obtained.

3. Results and discussion

In Fig. 1, we present the minimum interface trap density values, obtained from the C–V measurements, as a function of the time at which the samples have been exposed to the cleaning plasma. The other plasma cleaning conditions were 60 W and 0.54 mTorr (9.44 sccm). To compare these results to those obtained with the conventional wet-etching, we include the results at 0 s plasma exposure, which are the results obtained without plasma cleaning. As is observed in this figure, when the cleaning discharge exposure time increases up to 30 s, the minimum D_{it} value ($D_{it\,min}$) is significantly reduced. However, longer exposure times are deleterious for the interface behaviour, as shown in Fig. 1.

In Fig. 2, we present the resistivity and breakdown field values of the SiN_x:H gate insulator for the same samples whose results are shown in Fig. 1. The best values are obtained for the same exposure times of the cleaning plasma at which the best interface characteristics have been obtained. Again, longer exposure times damage the resistivity and breakdown field behaviour.

According to the previous figures, we can conclude that the best cleaning time is 30 s. Higher microwave powers and higher pressures have also been analysed, but they always decrease the SiN_x:H/InP interface performance.

The interface and bulk insulator property improvements indicate the reduction of the trap states at the interface under study. This fact may be attributed to three possible actions of the cleaning plasma: (a) surface cleaning, i.e., the N_2 plasma may remove the contaminant species (O_2 and C) detected on these samples by Auger measurements; (b) N passivation of the surface defects. This N passivation would consist of the filling of P vacancies (V_p) present at the InP surface. This passivation has been reported in previous works [7,8], where SiN_x:H/InP interfaces have been improved using N-rich nitrides due to a possible V_p passivation with N atoms coming from the insulator; (c) formation of P–N or In–P–N complexes during the plasma cleaning. The creation of these complexes has been recently analysed

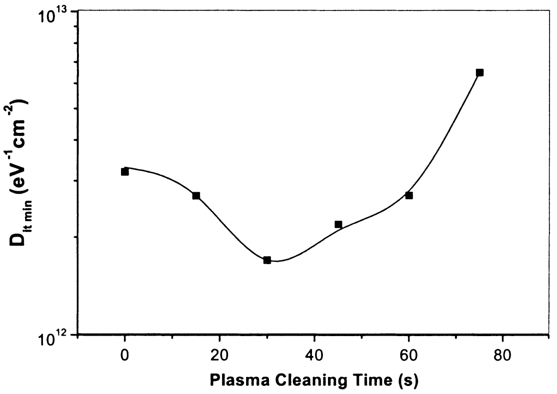

Fig. 1. Minimum D_{it} values of the trap density distributions obtained for different cleaning plasma exposure times, at constant pressure (0.54 mTorr) and power (60 W).

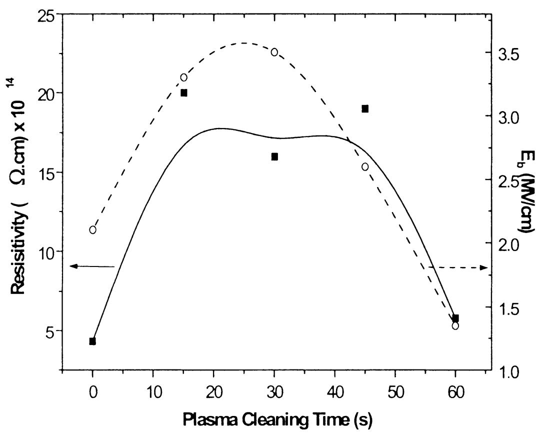

Fig. 2. Resistivity and breakdown field values obtained for different cleaning plasma exposure times at a constant pressure (0.54 mTorr) and power (60 W).

by Losurdo et al. [9] and they conclude that these P-nitrides are the main component of the nitride surface layer.

Longer exposure times or higher power plasmas induce considerable damage at both the interface and the insulator properties, probably due to a high ion bombardment that degrades the interface structure due to a great loss of P atoms. This hypothesis is under investigation by deep level transient spectroscopy (DLTS) measurements. Otherwise, for power levels below 60 W, it was difficult to excite the N_2 plasma.

After establishing the best N_2 plasma conditions, we have tried to improve the electrical behaviour of these structures performing a rapid thermal annealing (RTA) at the SiN_x:H/InP structure after the insulator deposition process. According to our previous studies [8,12], the best RTA process for an insulator composition of $x = 1.55$ is 500°C/30 s.

In Fig. 3, we show a comparison of the minimum D_{it} values obtained for the plasma cleaned sample, as well as the plasma cleaned and annealed sample. In this figure, we also include the minimum D_{it} value of a sample without any plasma or annealing treatment. As we can see, the thermal process does not improve the insulator–semiconductor interface as it could be expected according to previous results.

Attending to the third possible action of the plasma cleaning on the InP surface mentioned above, some authors have reported that due to V elements being volatile, the compounds formed with a V element and an N atom (V–N) are also volatile and thermally desorbed from the surface between 330°C and 530°C [9–11].

However, this plasma and thermal treatment sample show better interface characteristics than the one without any treatment. This fact can indicate that although the thermal process breaks the P–N bonds formed during the plasma cleaning, some N atoms can be thermally activated and occupy phosphorus vacancies, partially passivating the InP surface.

In Fig. 4, we present the resistivity and breakdown field values of the SiN_x:H gate insulator for the same samples that in Fig. 3. The best values are obtained again for the sample just cleaned with plasma, and it can be seen that the thermal annealing on the plasma-cleaned sample also decreases the insulator electrical properties.

As a final test, we have made a MIS structure with an O_2 plasma treatment to compare with the N_2 plasma results previously shown.

In Fig. 5, *CV* characteristics obtained for N_2 and O_2 plasma cleanings are compared. These treatments have

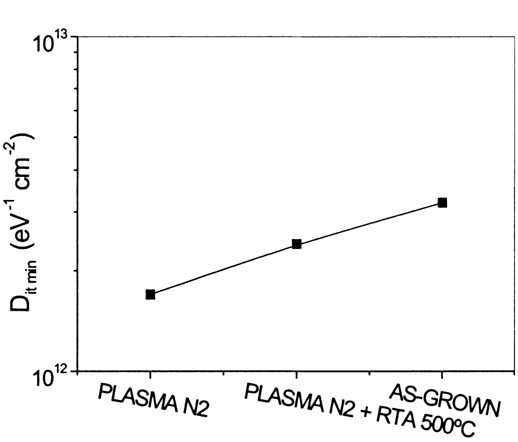

Fig. 3. Comparison of the minimum D_{it} values of the trap density distributions obtained for samples without plasma cleaning, with the best plasma cleaning and with plasma cleaning and RTA (500°C/30 s).

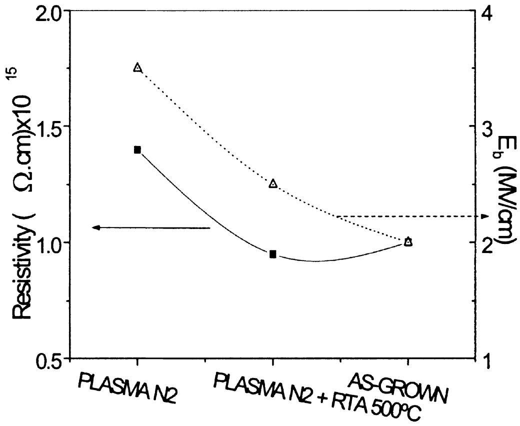

Fig. 4. Comparison of the resistivity and breakdown field values obtained for samples without plasma cleaning, with the best plasma cleaning and with plasma cleaning and RTA (500°C/30 s).

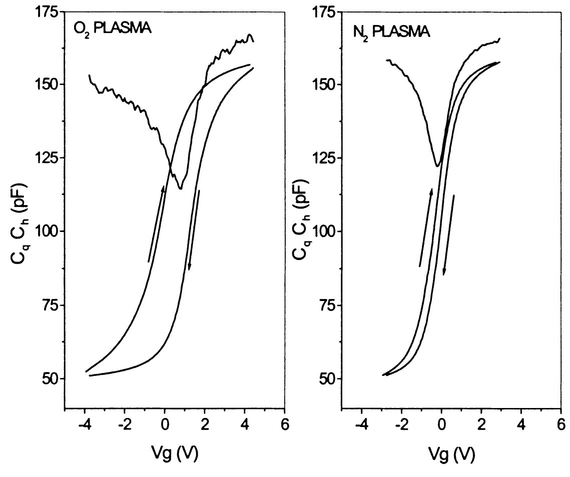

Fig. 5. Comparison of the *CV* characteristics for samples cleaned with O_2 and N_2 plasma (exposure time: 30 s; power: 60 W; pressure: 0.54 mTorr).

been performed using the best plasma conditions studied before, i.e. 30 s of exposure time, 60 W plasma power and 0.54 mTorr pressure. As can be seen, O_2 plasma cleaning induces a large number of slow interface states, which produce an important hysteresis phenomenon. These slow states are probably related to the oxidation induced by this plasma cleaning.

4. Conclusions

Summarising, we have proved that 30 s low-power N_2 plasma cleans and passives the insulator/InP surface, improving the electrical performance of the metal–insulator–semiconductor Al/SiN_x:H/InP devices. This is probably due to the formation of N–P or In–N–P complexes that passivate the InP surface. Neither the thermal treatment after the N_2 plasma cleaning nor the use of other plasma gases such as O_2, improves the electrical behaviour of the Al/SiN_x:H/InP MIS structures.

Acknowledgements

The authors would like to thank CAI de Implantación Iónica from the Complutense University in Madrid for technical assistance with the ECR-CVD system. This research was partially supported by the Spanish government under Grant no. TIC 98/0740.

References

[1] Okamura M, Kobayashi T. Jpn J Appl Phys 1980;19(11):2143.
[2] Guivarc'h A, L'Haridon H, Pelous G, Hollinger G, Poertosa P. Appl Phys Lett 1984;55:1139.
[3] Averbeck R, Riechert H, Schlotterer H, Weinmann G. Appl Phys Lett 1991;59:1732.
[4] Mangot PS, Soukiassian P, Huttel Y, Hurkych Z, Gruzza B, Porte A. Appl Phys Lett 1993;63:1957.
[5] Gallet D, Hollinger G, Santinelli C, Goldstein L. J Vac Sci Technol B 1992;10(4):1267.
[6] Hu YZ, Joseph J, Irene A. J Vac Sci Technol B 1994;12(2):540.
[7] García S, Mártil I, González-Díaz G, Fernandez M. Semicond Sci Technol 1997;12:1650.
[8] Redondo E, Blanco N, Mártil I, González-Díaz G, Pelaez R, Dueñas S, Castán H. J Vac Sci Technol A 1999;17(4):2178.
[9] Losurdo M, Capezzuto P, Bruno G, Leo G, Irene EA. J Vac Sci Technol A 1999;17(4):2194.
[10] Hashizume T. Appl Phys Lett 1999;75(5):615.
[11] Astito A, Fourcaran A, Bastide G, Rouzeyre M, Leclercq JL, Durand J. J Appl Phys 1991;70(5):2584.
[12] Redondo E, Blanco MN, Mártil I, González-Díaz G, Fernandez M, Proc CDE-99 Cong. Madrid, June 1999. p. 381.