Electrical characterization of ECR enhaced deposited silicon nitride bilayers for high quality Al/SiN_x/InP MIS structure fabrication

S. DUEÑAS, R. PELÁEZ, E. CASTÁN, R. PINACHO, L. QUINTANILLA, J. BARBOLLA
Departamento de Electricidad y Electrónica, Escuela de Tecnologías de la Información, Campus "Miguel Delibes", Universidad de Valladolid, 47011 Valladolid, Spain
E-mail: sduenas@ele.uva.es

I. MÁRTIL, E. REDONDO, G. GONZÁLEZ-DÍAZ
Departamento de Física Aplicada III, Facultad de Ciencias, Universidad Complutense de Madrid, 28040 Madrid, Spain

The interfacial state density existing in metal-insulator-semiconductor (MIS) structures was measured by deep level transient spectroscopy technique. The MIS structures were fabricated on InP substrates by direct deposition of silicon nitride (SiN_xH) thin films by the electron cyclotron resonance method. In this work, we show that interfacial state density can be diminished without degrading electrical insulator properties by fabricating MIS structures based on a bi-layered insulator with different insulator compositions and different thickness. The effect of rapid thermal annealing treatment has been analysed in detail in these samples. An interface state density as low as $3 \times 10^{11}\,cm^{-2}\,eV^{-1}$ was measured in some structures.

1. Introduction

Indium phosphide is known to have low surface recombination velocity [1] and low density of surface states [2], which are important parameters to avoid the detrimental effects of interface trap densities on the device performance. However, some problems related to interfacial traps still remain in InP metal-insulator-semiconductor based devices. Interfacial traps are responsible for current drift in InP MISFETs [3–5]. Traps in the interfacial region cause undesirable current leakage, shift in threshold voltages, and reductions in the trasconductance of MISFETs.

Silicon nitride layers have been extensively used as gate dielectrics in thin film transistors (TFTs) [6, 7] as interlayer dielectrics in metal-nitride-oxide-Si (MNOS) devices, and as final passivation layers in integrated circuits. SiN_x films are typically fabricated either by plasma enhanced chemical vapour deposition (PECVD) or low-pressure chemical vapour deposition (LPCVD) methods. In the current work, the electron cyclotron resonance (ECR) plasma method [8] was used. Due to the low ion energies ($<25\,eV$) in the ECR plasma [9], this deposition technique allows "soft" conditions to be created during deposition. Nitride films were deposited as a function of the gas flow ratio, $R = [N_2]/[SiH_4]$. Total flow rate was modified to vary the insulator stoichiometry, that is, the nitrogen content in the SiN_x layers which was denoted as x.

In a previous study [10, 11], we investigated the influence of the nitrogen content on the insulator film properties. An inverse correlation between the insulator composition and the density of interface traps was observed. The minimum trap density concentration was obtained for films with the maximum [N]/[Si] ratio, $R = 9$, corresponding to $x = 1.49$, i.e. high nitrogen content in the insulator. The decrease of interfacial defects as the insulator stoichiometry was modified was explained in terms of a substitutional mechanism: N atoms coming from the insulator may be located at phosphorus vacancies, V_P, giving rise to N_{V_P} configurations.

However, the dielectric behaviour was not optimum for this concentration value because of the low values of resistivity, and its breakdown electric field. Nevertheless, when the nitrogen content was decreased ($x = 1.41$), these problems were reduced, and resistivity and breakdown electric field became higher. As a conclusion, although a high nitrogen content insulator favors low interfacial state density, the electrical properties are simultaneously degraded. A reverse behaviour is detected for low nitrogen content insulator layers, where the electrical properties improved, whereas the interfacial trap density increased.

The aim of this work is to experimentally prove that MIS structures based on bi-layered insulators with different compositions and thickness show improvements both in their interface traps density and in their electrical properties.

2. Sample description

The substrates used in this work were undoped n-type LEC grown InP with an unintentional dopant concentration of $5 \times 10^{15}\,cm^{-3}$. The metal-insulator-semi-

0957–4522

conductor structures were fabricated by directly depositing silicon nitride films on InP wafers by the electron cyclotron resonance (ECR) plasma method. The deposition temperature was 200 °C.

The devices were fabricated as follows: prior to the insulator deposition, wafers were cleaned with organic solvents, and the native oxides were stripped. Subsequently, samples were transferred to the insulator deposition chamber. This consists of a home-made vacuum chamber attached to an ECR reactor. The deposition was carried out with the following parameters: substrate temperature (200 °C) and total pressure (0.08 Pa) were held constant for all the experiments. Microwave power was also kept constant at 100 W. Two gases were used: N_2 for generating the plasma, and pure SiH_4.

The value of gases flux ratio, $R = [N_2]/[SiH_4]$, was varied from 5 $(x = 1.41)$ to 9 $(x = 1.49)$ and the deposition time was scaled to obtain insulator films with different thicknesses. MIS structures based on single-layered and bi-layered insulators have been fabricated in order to compare the experimental results. The bi-layered insulator is fabricated as follows: first, an insulator film is grown on the InP, with $x = 1.49$ to minimize the interfacial state density and, then, a second one was deposited with $x = 1.41$ to improve its electrical properties. Two groups of bi-layered insulator MIS structures were fabricated differing in the total thickness of the insulator layer: 50 nm and 20 nm. For the first group, the thickness of the bottom layer $(x = 1.49)$ was 10 nm and that of the top layer $(x = 1.41)$ was 40 nm. For the 20 nm bi-layered insulator samples, the values were 5 and 15 nm, respectively. Rapid thermal annealing (RTA) treatments of 30 s at different temperatures ranging from 400 to 800 °C were carried out. Ohmic contacts for the InP and SiN_x : H layers were produced using evaporated AuGe/Au and Al, respectively, alloyed at 300 °C for 20 min.

Finally, we have fabricated a complete series of single-layered insulator with 50 nm of insulator thickness – corresponding to the insulator stoichiometry of $x = 1.49$ – as control samples, which were also annealed using the same RTA conditions.

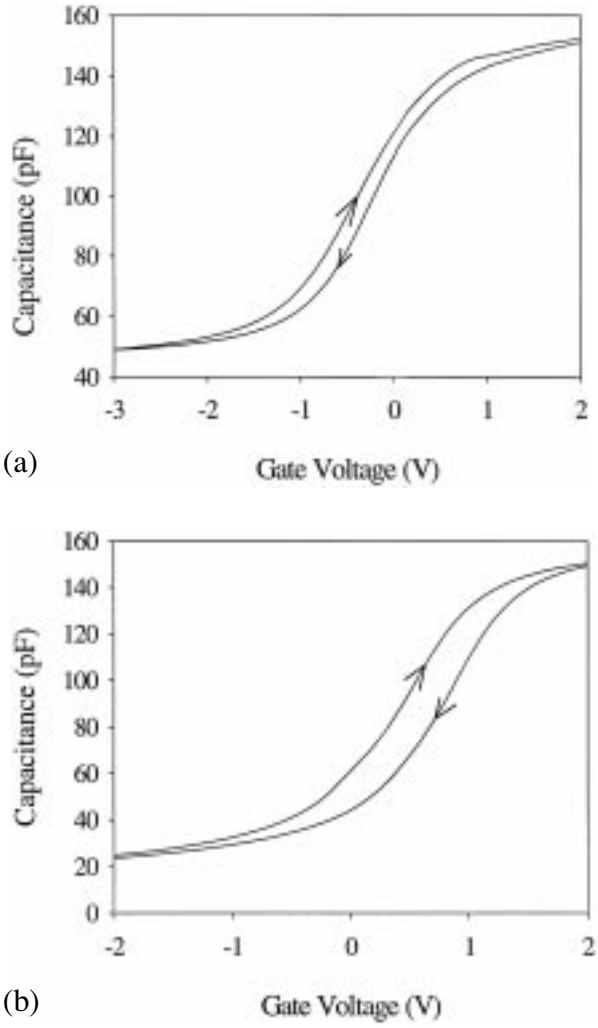

Figure 1 Capacitance–voltage curves for MIS structures based on bi-layered insulator with 50 nm total thickness insulator annealed at 400 °C (a) at room temperature, and (b) at $T = 78$ K. Curves have been carried out with two different voltage scan directions.

3. Experimental results and discussion

C–V measurements were carried out at room temperature and at a temperature of 78 K, putting the sample in a light-tight, electrically shielded box. The measurement set up involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer both of which were microcomputer controlled. Fig. 1a shows the 1 MHz-capacitance-voltage $(C–V)$ curves at room temperature for the bi-layered insulator sample with a total insulator thickness of 50 nm. As can be seen, these curves show hysteresis phenomena. This behaviour has been previously reported by Lau *et al.* [12] and may be understood by the defect model suggested by Hasegawa *et al.* [13, 14]. These authors proposed that the interface states are distributed both in energy and in space. This distribution is called disorder-induced gap-state (DIGS) continuum. Emission and capture of free electrons by states located far from the interface can occur by means of tunneling mechanisms. Therefore, since these processes are tunnelling-assisted, they are slow and non-symmetrical. In consequence, the experimental capacitance values depend both on the direction and on the speed of the voltage variation and, thus, hysteresis effects are observed.

In Fig. 1b, 1 MHz *C–V* curves at 78 K are plotted for the same sample. We can observe that these curves are different from those recorded at room temperature. A flat band voltage displacement to less negative values and a stretch-out of curves are observed. This experimental result suggests that some traps in the material are frozen at low temperatures. The hysteresis phenomenum can be observed at this temperature too. This behaviour has been observed for all the samples analysed in this work, and the results obtained were quite similar to those which are showed here.

The devices were also characterized by deep level transient spectroscopy (DLTS) measurements between 78 K and 300 K. These measurements were carried out by using a 1 MHz Boonton capacitance meter and a HP 54501A digital oscilloscope to record the capacitance transients. A Keithley 617 programmable electrometer and a HP 214 pulse generator were used to introduce the quiescent bias and the filling pulses, respectively. The

pulse width was selected as 10 ms to completely fill up traps. The D_{it} distribution was deduced from DLTS measurements with the method described by Yamasaki *et al*. [15]. No conductance versus frequency measurements have been used to determine D_{it} due to the existence of ''slow'' traps in the insulator. We have recently proved [16] that the charge–discharge transients of these ''slow'' traps makes it difficult to correlate the conductance measurements with DLTS results. These traps are considered to be different from the ''fast'' interface-state continuum localized at the interface which causes frequency dispersion of MIS capacitance [17].

In Fig. 2, we have plotted the D_{it} distribution obtained from DLTS measurements for the devices with different insulator compositions described before. The presence of a maximum located at about 0.2 eV below the edge of the conduction band is detected. This peak has been found in some of the samples in our study. For instance, it appears in the samples submitted to an RTA treatment at 500 and 600 °C. This trap has been associated with a deep level because its height and position do not change with polarization (several measurements with different saturating pulses and with different bias voltage were carried out). The identity and physical origin of this trap is now under investigation.

At room temperature, an increase in the DLTS signal value has also been observed, which may be related to the presence of a discrete-level near the midgap in the D_{it} profiles. This peak can be related to the fact that the capture of thermally generated holes becomes faster than the emission of electrons for states deeper than a threshold energy.

In this study, we focus our attention on the evolution of interfacial state density with the insulator composition and with the RTA temperature in order to obtain further insight into its physical nature.

D_{it} profiles have been plotted in Fig. 2 for the three series of samples. The dependence of D_{it} profiles on the RTA temperature follows the same trend for the three series of samples. As can be observed, D_{it} profiles decrease for samples annealed at temperatures of 400 and 500 °C, whereas the interfacial damage increases for the samples annealed at temperatures higher than 500 °C.

Some differences in the interfacial state density value must be pointed out for each group of samples. This parameter is kept in the range of $1-8\times10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ for the single-layered sample (Fig. 2a). However, for the bi-layered samples with 50 nm total insulator thickness, a lower interfacial state density than the previous one is detected, and D_{it} remains in the range of $0.4-2\times10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ (Fig. 2b). Finally, for the bi-layered samples with 20 nm total insulator thickness, the lowest interfacial traps density obtained is in the range of $0.3-4\times10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ (Fig. 2c). Therefore, we can conclude that the interfacial state density has been improved, i.e. decreased, for these bi-layered structures.

On the other hand, as for the electrical insulator properties of the analysed samples, they are improved in the MIS structures based on the bi-layer insulator. Electrical properties of the films – such as, resistivity, ρ, and breakdown field, E_B – were obtained by measuring the *I–V* characteristics of the MIS structures. The resistivity was obtained at an electric field of 1 Mv/cm [18]. The value of E_B was obtained as the field at which the MIS current reaches 1 μA/cm^2 [12]. The bi-layered structures with 50 nm of insulator thickness exhibited the better values of the electrical properties – i.e. a resistivity of $2.6\times10^{14}\,\Omega\,\mathrm{cm}$, and a breakdown electric field of

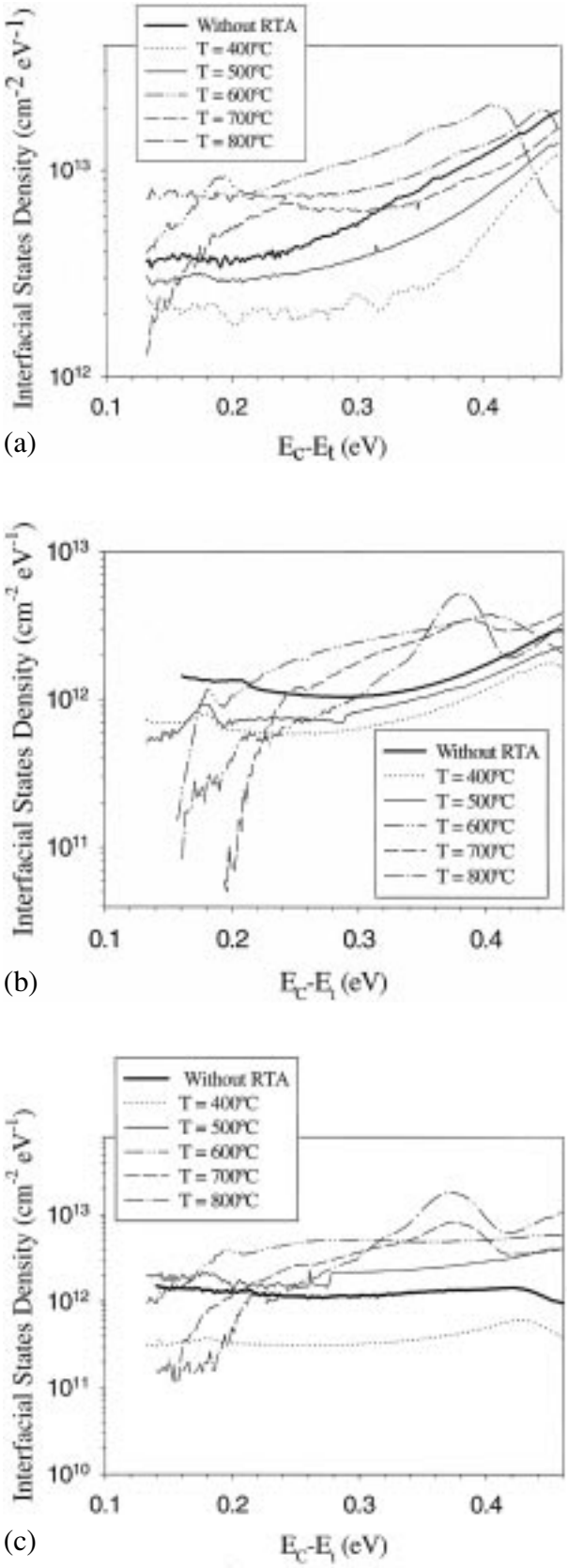

Figure 2 Interfacial state density measured by DLTS technique for: (a) single-layered insulator (control) samples, (b) bi-layered insulator samples with 50 nm total insulator thickness and (c) bi-layered insulator samples with 20 nm total insulator thickness.

1.7 MV/cm. Poorer values were obtained for the single-layered samples, $\rho = 6 \times 10^{13}\,\Omega\,\text{cm}$, and $E_B = 1.2$ MV/cm.

In Fig. 3, the dependence of D_{it} on RTA temperature is represented, for the bi-layered samples of 50 nm, and for the single-layered (control) samples. Thermal treatment causes a decrease in the interfacial state density when annealing temperature remains below 500 °C, but, beyond this temperature, D_{it} increases. In consequence, a minimum in D_{it} is observed corresponding to samples which have undergone an RTA treatment at 500 °C.

The following tentative explanation can be suggested. The surface of InP becomes defective of the most volatile element (phosphorus), when such a surface is chemically cleaned or plasma exposed. Even in the case of remote plasma exposure, such as an ECR type, a loss of P has been reported [10]. Therefore, a defective surface is generated where phosphorus P vacancies (V_P) are present, making the semiconductor unable to be applied in electronic devices, e.g. FETs, where the surface quality is a critical issue. Since ECR is a remote plasma method, the induced amount of V_P should remain much lower than that obtained by direct plasma methods.

When a low temperature RTA treatment is applied to the sample, some intermixing between the insulator and the semiconductor surface takes place [10]. In particular, nitrogen atoms of the insulator move towards the first atomic layers of the semiconductor surface. As a consequence, N atoms coming from the insulator may occupy phosphorus vacancies, V_P giving place to N_{V_P} configurations. Thus, the interfacial state density decreases because the phosphorus vacancies density does, due to its effective passivation produced by N atoms. On the other hand, when a high temperature RTA treatment is applied, the evolution is different. It has been proved in a previous study [19, 20] that a loss of nitrogen takes place at annealing temperatures higher than 500 °C. Thus, the V_P passivation by N atoms is diminished, increasing the V_P concentration, and, in consequence, the interfacial trap density increases.

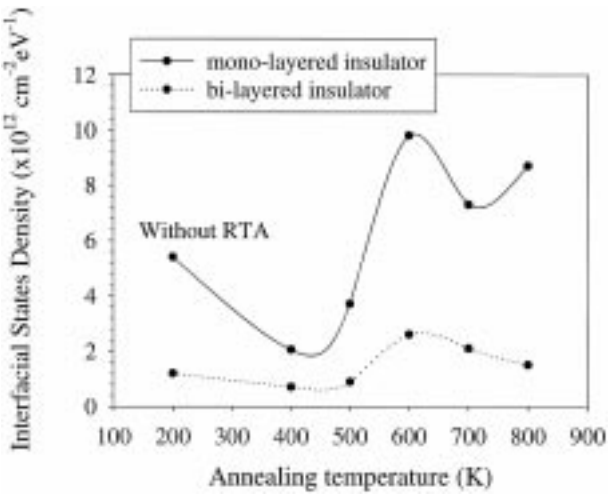

Figure 3 Interfacial state density as a function of RTA temperature for the single-layered insulator samples and for the bi-layered insulator sample with 50 nm total insulator thickness. D_{it} has been measured at a fixed energy from the conduction band. The unannealed sample is placed at 200 °C because the processing temperature during the ECR process was fixed at 200 °C.

It might be suggested that RTA treatment gives rise to two simultaneous and opposite processes, whose balance is temperature-controlled. For the lower annealing temperatures, below 500 °C, the V_P passivation effect is dominant, causing D_{it} to decrease. For annealing temperatures higher than 500 °C, the nitrogen loss from the phosphorus vacancies dominates, decreasing the above passivation and, as a result, D_{it} increases.

4. Conclusions

MIS structures obtained by deposition of $SiN_x \cdot H$ bi-layers by the ECR method on InP wafers were fabricated and subsequently rapid thermal annealed at different temperatures. These samples were characterized in detail by the correlation of three electrical techniques: *I–V*, *C–V*, and DLTS. In particular, electrical insulator properties, such as resistivity, ρ, and electrical breakdown field, E_B, and interfacial state density were measured.

The aim of this work is to prove experimentally that MIS structures based on bi-layered insulator with different compositions and thickness show improvements both in their interface trap density and in their electrical properties.

Hysteresis phenomena were observed in *C–V* curves both at room temperature and at 78 K, which suggested that traps exist in the material. D_{it} profiles for the bi-layered samples of 20 nm total insulator thickness presented the lowest values, remaining in the range of $0.3\text{–}4 \times 10^{12}\,\text{cm}^{-2}\,\text{eV}^{-1}$. Higher values were obtained for the bi-layered sample of 50 nm total insulator thickness, which were in the range of 0.4–$2 \times 10^{12}\,\text{cm}^{-2}\,\text{eV}^{-1}$. Finally, the highest values of D_{lt} were measured in the single-layered insulator samples ($1\text{–}8 \times 10^{12}\,\text{cm}^{-2}\,\text{eV}^{-1}$). As for the insulator electrical properties, the optimal values were measured for the bi-layered insulator samples – such as a resistivity of $2.6 \times 10^{14}\,\Omega\,\text{cm}$; and an electric breakdown field of 1.7 MV/cm. Poorer values were obtained for the single-layered samples: $\rho = 6 \times 10^{13}\,\Omega\,\text{cm}$, and $E_B = 1.2$ MV/cm.

The dependence of D_{it} on the RTA temperature has been also studied. Thermal treatment causes a decrease in the interfacial state density when the annealing temperature remains below 500 °C, but, beyond this temperature, D_{it} increases. In consequence, a minimum in D_{it} is observed corresponding to samples which have undergone an RTA treatment at 500 °C. A tentative explanation of this behaviour has been proposed here.

References

1. H. C. CASEY, Jr. and E. BUEHLER, *Appl. Phys. Lett.* **30** (1977) 247.
2. L. G. MEINERS, *J. Vac. Sci. Technol.* **19** (1981) 373.
3. M. OKAMURA and T. KOBAYASHI, *Jpn. J. Appl. Phys.* **19** (1980) 2143.
4. D. FRITZSCHE, *Inst. Phys. Conf. Ser.* **50** (1980) 258.
5. D. L. LILE and M. J. TAYLOR, *J. Appl. Phys.* **54** (1983) 260.
6. L. HE and G. LUCOVSKY, *Mater. Res. Soc. Symp. Proc.* **336** (1994) 787.
7. J. KANICKI, F. R. LIBSCH, J. GRIFFTH and R. POLASTRE, *J. Appl. Phys.* **6** (1991) 2339.
8. S. SITBON, M. C. HUGON, B. AGINS, F. ABEL, J. L.

COURANT and M. PUECH, *J. Vac Sci. Technol. A* **13** (1995) 2900.
9. A. KAPILA, X. SI and V. MALHORA, *Appl. Phys. Lett.* **62** (1993) 2259.
10. S. GARCÍA, I. MÁRTIL, G. GONZÁLEZ DÍAZ, E. CASTÁN and S. DUEÑAS, *J. Appl. Phys.* **83** (1998) 600.
11. *Idem.*, *ibid.* **83** (1998) 332.
12. W. S. LAU, S. J. FONASH and J. KANICKI, *ibid.* **66** (1989) 2765.
13. L. HE, H. HASEGAWA, T. SAWADA and H. OHNO, *ibid.* **63** (1988) 2120.
14. *Idem.*, *Jpn. J. Appl. Phys.* **27** (1988) 512.
15. K. YAMASAKI, M. YOSHIDA and T. SUGANO, *ibid.* **18** (1979) 113.
16. M. MAEDA and Y. ARITA, *J. Appl. Phys.* **53** (1982) 6852.
17. S. DUEÑAS, R. PELÁEZ, E. CASTÁN, R. PINACHO, L. QUINTANILLA, J. BARBOLLA, I. MÁRTIL and G. GONZÁLEZ-DÍAZ, *Appl. Phys. Lett.* **71** (1997) 826.
18. E. H. NICOLLIAN and A. GOETZBERGER, *Bell. Syst. Tech. J.* **46** (1967) 1055.
19. F. L. MARTÍNEZ, I. MÁRTIL, G. GONZÁLEZ-DÍAZ, A. M. BERNAL-OLIVA, E. MÁRQUEZ, B. SELLE and I. SIEBER (submitted).
20. F. L. MARTÍNEZ, I. MÁRTIL, G. GONZÁLEZ-DÍAZ, B. SELLE and I. SIEBER (submitted).

Received 14 September 1998
and accepted 17 December 1998