Defining a Strategy to Perform Life-Tests with Analog Devices

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***Abstract*—Unlike for memory elements inside integrated circuits, scarce life tests have been performed to study single event transients in discrete analog devices. The reason is that life tests require a large amount of samples to be stored for having enough data allowing statistical conclusions and, usually, single event transients are captured by means of oscilloscopes. In this paper, we propose a strategy to carry out life tests in analog voltage comparators by means of digital programmable device that can detect anomalous pulses in the voltage comparator. Besides, the idea on which this kind of tests relies can be extended to be used with other families of analog devices, such as operational amplifiers, voltage references, etc.**

***Index Terms*—Analog devices, field tests, life tests, voltage comparator.**

I. Introduction

TESTS to evaluate the tolerance of the electronic devices to single event effects are typically carried out by the following three procedures: Accelerated tests, pulsed-laser tests and life tests. Life tests, also known as field tests, consist in accumulating a large number of identical devices and leaving them working for some weeks, months or years. Periodically, a control system checks if some kind of error has occurred so that a statistical study be extracted.

Unfortunately, natural radiation fluence is very low so a huge number of devices is necessary to collect significant data. However, interesting results have arisen from life tests performed in ground or underground laboratories [1]–[8], in avionics [9]–[11], or in operative space satellites [12], [13].

Most of these works share an important characteristic: They describe experiments where the kind of single event was a bit-flip, either in pure SRAMs, in the cache memory of microprocessors, or in FPGAs. A pattern is written in the memory, this one is led to sleep mode, and read later. Discrepancies between the original and read words are logged, including the position of the word and the time of reading. The only exceptions are [3], which studied CCDs, and [12], mainly devoted to the study of SEUs/MBUs in SRAMs but with the ability of detecting single event latch-ups. Finally, a recent work by Arruego *et al.* [13] detects single event transients in an optical wireless system inside a satellite comparing its reading with that provided by a conventional wired device.

Single event transients (SET) in voltage comparators are known to be the ultimate reason of some electronic fails in satellites [14]–[16]. Since analog devices do not retain information, the single event transients vanish in a few microseconds without leaving any trace. Therefore, the strategy used to investigate memory systems cannot be applied. However, some devices such as the voltage comparators, the output of which is HIGH or LOW, can be used to bias the input of digital devices so the possible single event transients can be recorded for a statistical characterization.

In this paper, we propose how to implement a life test to investigate single event transients in this kind of analog devices. This strategy can be used to design specific boards that can be used to investigate the occurrence of this phenomenon in some natural radiation environments.

II. Capture of Single Event Transients

The proposed strategy consists in creating independent cells connected to the output of a voltage comparator, able to register any anomalous output switch, and a master that controls all of these cells. The only requirement for the single event transients to be detected is that, during the event, the output voltage must reach the opposite logic value.

A. The whole system

Let us suppose that we build a system of the structure shown in Fig. 1. This machine has the following blocks:

- **Capturers:** There is a set of *N+1* capturers (S00, S01, ...) working as slaves of the master. Every one has an input connected to the output of the external voltage comparators ready to detect any output flip. These devices can be reset by the master, and can inform the master that a single event transient has been detected along with its characteristics.
- **Master:** The master controls the set of slaves (resetting them or compiling the registered events), the communication with an external computer, and the backup of data. Besides, it has some kind of calendar to associate every event with a date and time.
- **Backup:** This is an optional block to store the data to prevent their loss in case of some power cuts, failures

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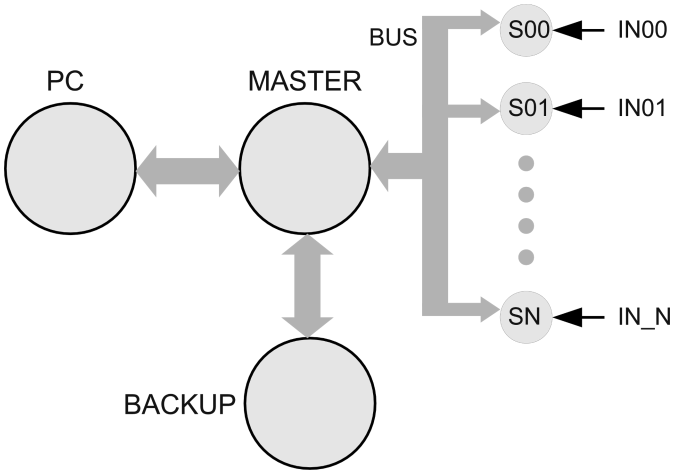

Fig. 1. Global schematics of the SET capture machine, ready to detect any spurious switch from **"1"** to **"0"** or vice versa.

of the master, etc. For instance, just a magnetoresistive random access memory (MRAM) or a phase-change RAM (PRAM) is enough since they are easy to write and read, non-volatile, and immune to data corruption by single events.

- **PC:** A computer provides an interface for human access to the main system. It recovers data from the machine and allows the scientist to initialize the system.

Master and capturers are synchronous blocks controlled by an external clock, which is not included in Fig. 1. The selection of the clock frequency is crucial since, as it will be seen, the lower the clock period, the better the SET description.

B. State machine of the slaves/capturers

The behavior of the slaves (S00, S01, ...) and their communication with the master can be explained by means of a state machine. The state machine of the capturers is summarized in Fig. 2. In this figure, the stable output of the voltage comparator is supposed to be **"1"** although minor changes in the state machine are required to detect switches from **"0"** to **"1"**.

The machine has got, at least, two input signals: An input coming from the voltage comparator and a reset coming from the master. The way of working is the following:

1) **Watch:** The machine continuously tracks the value of the signal coming from the external voltage comparator and only quits if its value is not the nominal one. A variable, called "Duration" (*D* in Fig. 2) is set to **"0"**.
2) **Count:** This state is reached if an anomaly appears in the input signal. While the input signal is not the nominal value, the state is not left until the input signal recovers its original value. Following each clock cycle, the value of D is increased so the transient duration can be estimated in units of clock period.
3) **Send:** The capturer informs the master that an SET has been observed and sends the transient characteristics to the master. Some alternatives not included in the graph can be implemented. E. g., the slave can trigger an internal signal to draw the attention of the master. Or, more simple, just wait a periodical scan of the capturers performed by the master. Actually, this state just represents a chain of secondary states, the purpose of which is holding the transient characteristics and sending them to the master.
4) **Wait:** Once the capturer has sent the information to the master, it waits for a RESET signal to return to the Watch state. The existence of this signal simplifies the implementation of the state machine but it is not absolutely necessary.

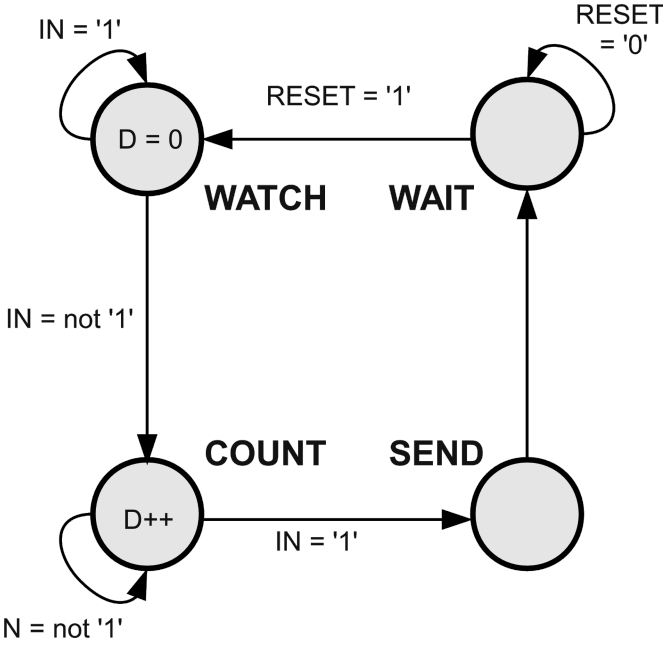

Fig. 2. State machine of the slaves/capturers. This machine is ready to detect anomalous switches from **"1"** to **"0"**. **IN** and **RESET** are external signals.

Actually, the kernel of the state machine is the first pair of states. The other are just a simplification of the procedure followed by the capture to send safely the data to the master. Besides, as every slave is independent of each other, it is not compulsory that all of them detect the same kind of single event transient. Thus, slaves ready to detect **"1"** to **"0"** pulses can coexist with other slaves that are triggered by the opposite transient (**"0"** to **"1"**).

III. Implementation in microprocessors

The state machine depicted in Section II can be easily adapted to the use of microprocessors. In fact, the transition from the WAIT state to COUNT when the input value changes is equivalent to an external interrupt in specific input pins of a microprocessor.

A. Code in C language

Thus, the state machine was implemented in a PIC18F2423 working with a 20-MHz clock. This device was selected since it is a low-cost microprocessor and that can be programmed in a dialect of C language (Exactly, in the CCS C language [17]) very easy to follow by most of the readers. However,

the strategy can be exported to whichever microprocessor we may prefer. Given that the program inside the microprocessor was developed in C language, the master in Fig. 1 was just the `main()` routine. In this routine, a calendar was implemented using a delay on the order of 1 s inside an infinite loop. Thus, the microprocessor could know how many seconds, minutes, hours, ... had elapsed since the power-up. Communication with the computer and the backup of data, if necessary, were elementary.

The microprocessor has several pins to activate external interrupts. During the execution of the interrupt subroutine, a counter can be initialized and stopped once the transient has vanished. For instance, the pin B0, which is the bit 0 of the B port, can be programmed as follows to detect if the output of the comparator quits a nominal value of **"1"**.

```
#int_EXT
void  EXT_isr(void)
{
   set_timer0(0x0000);
   do{ }while (input(pin_b0)!= TRUE);
   setup_timer_0(RTCC_OFF);
   duration = get_timer0();
   setup_timer_0(RTCC_INTERNAL);

//duration is 16-bit wide and must be
//split into two bytes
   duration_L = (char) duration%256;
   duration_H = (char) ((duration-
     (unsigned int16) duration_L)/256);

//SET data are registered, including
//the port where the SET was detected,
//its duration and the event date.

    SET_port[number_sets]=0;
    SET_month[number_sets]=month;
    SET_day[number_sets]=day;
    SET_hour[number_sets]=hour;
    SET_minute[number_sets]=minute;
    SET_second[number_sets]=second;
    SET_duration_H[number_sets]=
        duration_H;
    SET_duration_L[number_sets]=
        duration_L;

//The device only can detect up
//to number_max_sets SETs.
    if (number_sets < (number_max_sets-1))
       {number_sets++;}
}
```

In this subroutine, *number_sets* is the number of SETs that has been detected before the trigger of the subroutine. It is defined as a global variable, shared by all of the interrupt routines, and initialized to 0. *SET_xxx[k]* is an array to register the characteristics of the single event transient (Input port where it was detected, the date and time, and the duration in clock cycles). Finally, *duration*, split into two variables, contains information about the transient duration.

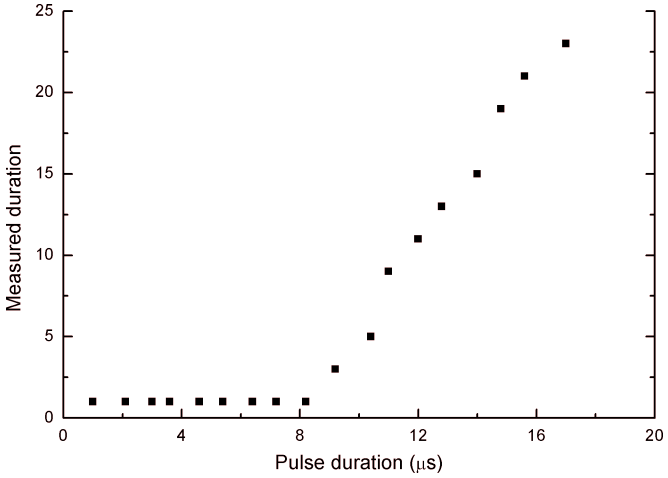

Fig. 3. Reading of the internal microprocessor counter vs. the transient duration. The clock frequency was 20 MHz.

Is this design effective? Fig. 3 shows the value of the internal counter of the microprocessor with different pulse durations if HIGH-TO-LOW transients are sought in the B0 pin. We can see that single event transients with a realistic duration of about 1 μs can be detected although the duration cannot be determined until the duration is on the order of 8 μs. This is not a realistic value in the case of voltage comparators but, in case of using much faster microprocessors, the transient duration can be measured in a better way.

B. Drawbacks of the microprocessor implementation

The main advantage of the microprocessors is that the state machine is easily implemented with a few lines of C language code. However, there are also some disadvantages that should be taken into consideration before developing an actual detector.

1) **Few input ports:** Microprocessors do not usually have a large number of inputs where the single event transient can be detected. E.g., in the PIC18F2423 there are only three inputs {B0, B1, B2} that detect signal edges. The B3-B7 inputs can be combined to create an additional external interrupt but, at any rate, there would be only four available inputs. However, this factor strongly depends on the nature of the selected microprocessor.
2) **Slow response:** There is always a delay between the interrupt and the execution of the procedure. This leads to an incorrect estimation of the SET duration shown in Fig. 3. Thus, the microprocessor behaves correctly only for the longest duration of pulse (in this case, with a 20-MHz clock, over 8 μs).
3) **Calibration:** The measured duration of identical pulses can be slightly different depending on the input pin. Therefore, a previous calibration of each input pin is required.
4) **Reliability of the microprocessor:** The microprocessor itself can be affected by single events. Therefore, it is necessary to protect it against these problems. One

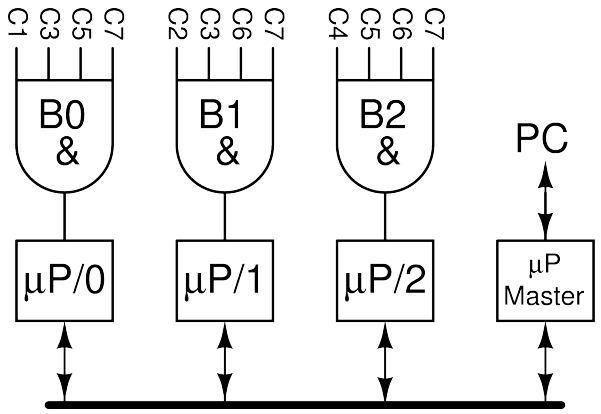

Fig. 4. Graph showing how to watch 7 comparators with 3 microprocessors and 1 master connected to the PC. The inputs of B0 are those comparators in which the bit 0 is **1** (1, 3, 5 & 7); To B1, the comparators in which the bit 1 is **1** (2, 3, 6 & 7), etc.

choice is using rad-hard devices or protecting the program code following techniques such as those shown in [18]. At any rate, the penalty is either a slower response or a cost increase.

The problem of the scarcity of input ports can be solved using interrupt controller cores. In fact, there are some well-known and tested VHDL blocks provided by FPGA manufacturers, such as Xilinx or Altera, that handle interrupts from a parallel bus. The main drawback of this choice is that all of the inputs converge to a sole output connected to the microprocessor. Therefore, we cannot know in which comparator the single event transient occurred.

A less sophisticated but easier to develop method is the use of combinational gates with a large number of inputs. Let us suppose that we have an electronic system consisting in:

- N AND gates with 2^{N-1} inputs each, $N \in \mathbb{N}$.
- $2^N - 1$ comparators with HIGH output voltage.
- N microprocessors, with an external interrupt pin connected to the output of each AND gate. This set of N devices is controlled by another microprocessor, called *master*.

Now, let us enumerate the AND gates from 0 to $N-1$ and every comparator from 1 to $2^N - 1$. Now, let us choose the j^{th} comparator, $j \in \left(1, 2^N - 1\right)$ and express it in binary format. Beginning with $k = 0$, let us proceed as follows: If the bit in k^{th} position is "1", the comparator ouput must be connected to an input of the k^{th} AND gate. If not, let us continue towards the $(k+1)^{th}$ position until $k = N$. Fig. 4 is an implementation of this algorithm with $N = 3$, so there are 7 comparators (C1, C2,.. C7) with HIGH output value and 3 AND gates and comparators.

It is important to highlight that the microprocessor contain an internal calendar to register the date and time when the single event transient was observed. Obviously, all of the N calendars are similar. Now, let us suppose that a single event transient occurs in one of the comparators, for example in the 3^{rd} one. Taking into account that the output of every AND gate is HIGH, the transient will be transmitted as a LOW spike to the B0 & B1 microprocessors, launching the interrupt routine but being absent in the B3 device. No other comparator can write this signature so, after inspecting the log file downloaded by the PC, we can deduce the time when the transient occured, its duration and, specially, in which comparator did.

The best way to implement the set of N AND gates is writing an VHDL design inside an FPGA or CPLD. Thus, it is not compulsory that all of the voltage comparators have HIGH outputs but and the system becomes more flexible. However, in case of deciding to use programmable device, it might be better to follow the strategy proposed in the next section.

IV. Implementation in FPGAs

The state machine depicted in Fig. 2 can be implemented by means of VHDL code inside an FPGA. Writing the code for this kind of devices is not much more difficult and, morover, comes along with the following advantages: First of all, the designer can devote as many input pins as possible to survey the output of the comparators. In fact, the design is modular and every input is controlled by an individual state machine. Therefore, unlike the microprocessors, there are not restrictions related to the inputs with enabled interrupts.

Besides, the FPGA can be easily protected against single event upsets with the insertion of triple modular redundancy (TMR) in the VHDL code of the device. Thus, a VHDL design with 64 capture cells controlled by a master and with states protected by TMR was designed and fitted in several typical low cost FPGAs. In particular, we focused in the Xilinx Spartan 3E-200 and Altera Ciclone III EP2C35F672C6N. They were chosen since they are found in typical development kits (Digilent BASYS, Altera DE2) and, although they are different from each other, both of them represent the cheap line of the mainstream manufacturers.

Unlike the C code reported in Section III-A, the VHDL code for the FPGAs is much longer (more code lines and several files in a tree organization). For the sake of brevity, it is not included in this paper.

In the case of the Xilinx devices, the 64-input VHDL code with TMR protection needed 27% of the available LUTs and the highest clock frequency calculated by the fitting software was 66.2 MHz. Given that the state machine shown in Fig. 2 is synchronous, the duration of the SETs must be, at least, the inverse of this value (∼15 ns) to detect the event. However, actual transients in voltage comparators are on the order of 1 μs or more so the detection is feasible.

Finally, the results obtained in the Altera device are even more interesting since the maximum clock frequency is 71 MHz although it could be even increased since it depends on the placement of the input pins. Besides, only 9 % of the available LUTs were used and several hundreds of input pins could be used to increase the number of analog comparators.

V. Extension to other devices

The strategy to detect single event transients depicted in the previous sections must accomplish an important requirement: However the analog device may work or be biased, it must offer a **stable** output voltage equal to one of the hard logic levels to be understood by the digital supervisor, either the

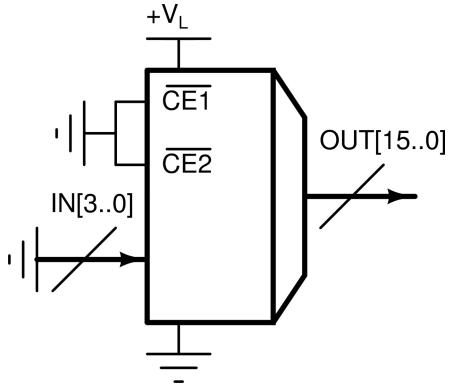

Fig. 5. A typical demux biased for life tests. The control inputs, with complementary logic, are tied to ground.

FPGA or the microprocessor. This is why the strategy has been mainly proposed for analog comparators, the output of which can be easily adapted to the appropriate output values.

Nevertheless, other devices could be tested following this strategy. Here are some of the possible candidates:

A. Combinational devices

This kind of devices lack of memory cells so only single event transients can occur. Besides, the values of the output voltage are compatible with the input requirements of the detectors. E.g., a demultiplexer, such as the 74HC154 or alike, can be tested disabling the output so that the output bus voltages are HIGH (Fig. 5). Thus, they can be connected to the detector.

However, it must be taken into account that if a transient occurs in the control logic block shared by all the outputs, there can be several simultaneous single event transients in the output bus. This does not commit the system in case of using an FPGA but is a serious drawback in the microprocessors since they can deal only with a unique interruption at the same time. A possible solution is using several microprocessors, joining each line of the bus to a different device. Later, comparing the date and time inside the microprocessor log, dumped to the PC, allows discovering how many outputs were affected.

B. Analog devices with resistors

Another possibility consists in the usage of resistors to achieve hard logic levels. Fig. 6 shows how to test an array of analog switches where pull-up or pull-down resistors allow creating compatible logic levels.

Another solution is using a couple of resistors as voltage divider. Thus, a voltage reference or a regulator can be tested as shown in Fig. 7. However, this solution has several disadvantages. First of all, the total power consumption increases to bias the resistors. Second, it is necessary that $V_{REF} > V_L$ so, e. g., negative voltage references are excluded. Finally, only output voltage drops are detected. In other words, if V_{REF} undergoes a spurious growth instead of a fall the transient cannot be observed by the detector.

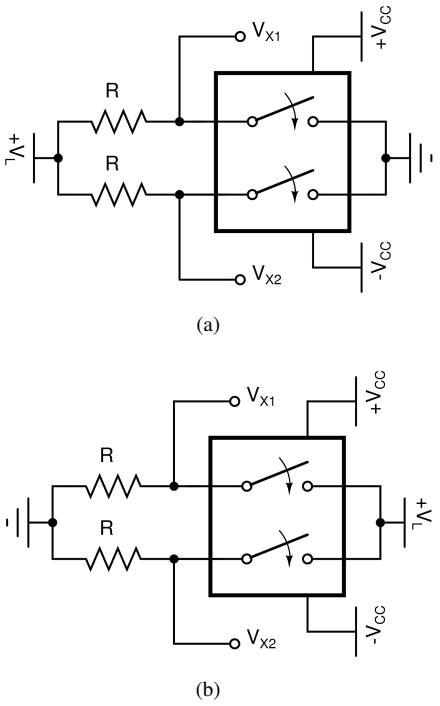

Fig. 6. Proposal of a test to detect sudden changes in the state of an analog switch. Supposing the switch open, the resistors work as pull-up (a) or pull-down (b). $V_{X,k}$ are connected to the detector

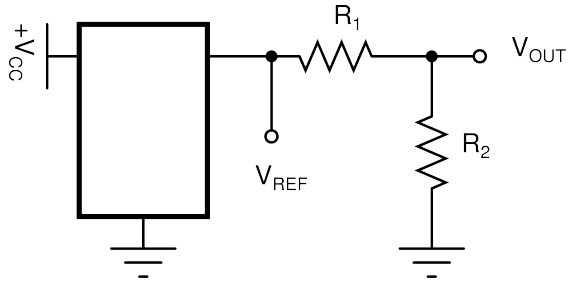

Fig. 7. Conversion of a reference voltage into a HIGH logic level. If V_L is the logic power supply value, $\frac{R_1}{R_2} = \frac{V_{REF}}{V_L} - 1$.

C. Trigger of comparators

An alternative solution consists in using analog comparators that survey if the output voltage of a target device exceeds some reference voltages. Fig. 8 is a simple example of how comparators can detect an analog transient occurring in the output of an operational amplifier, provided that this voltage go beyond a threshold level, ΔV.

This solution seems extremely simple and with an advantage that cannot be found in the other proposals: It can detect transients of different sizes. Thus, more comparators can be added to track the output of the operational amplifier, each one with a trigger level, ΔV_K.

Yet this solution also brings a lot of drawbacks. First of all, the more analog comparators, the more inputs in the detector is required which makes difficult the development of the protoboard containing the tested devices. Besides, bipolar transients or unipolar transients that trigger several comparators with different threshold voltages have the problem

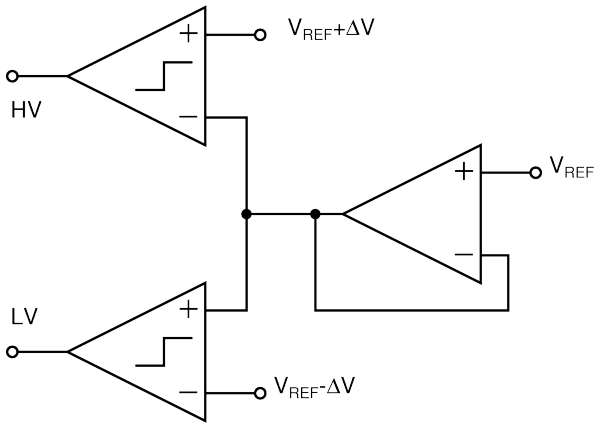

Fig. 8. A pair of voltage comparators that detect changes in the output of an operational amplifier larger than ΔV. The operational amplifier works as a voltage follower and LV & HV are connected to the detectors.

of almost simultaneous interrupts in microprocessors, such as that depicted in Section V-A.

In our opinion, the most significant drawback comes from the fact that the analog comparators are also liable to undergo single event transients. However, some additional details can minimize the significance of these unwanted events. Single event transients in comparator strongly depend on the input voltage difference since the cross section decreases two orders of magnitude or more in case of using voltage differences on the order of volts [19], [20]. Besides, common sense can help to discriminate some supposed events. E.g., if there are two comparators, with trigger levels of ΔV & $2 \cdot \Delta V$ and the latter detect an event but the former does not, we can conclude that the tested device did not undergo a single event but the surveying comparator. Another possibility is to build a life test for the comparators. If the designers build a protoboard based on Fig. 8 replacing the op amp by a constant reference voltage (e. g., ground if the output voltage of the op amps is supposed to be 0 V), a statistic study can be extracted to deduce the expected number of events associated with the tested op amps and with the comparators.

Another weak point is the reference voltages, V_{REF} & $V_{REF} \pm \Delta V_K$. They are provided by analog devices where single event can also occur. However, these reference signals are usually shared by several operational amplifiers so the log would show simultaneous events in all of the tested devices. This fact would help to identify the event as a failure of the references. Besides, the best way to build the trigger levels are by a chain of resistor in series joining a reference voltage and ground. Thus, the hazard of single event transients in the reference voltages is minimized.

VI. Conclusion

Life tests, also known as field tests, are experiments that investigate the influence of natural radiation on electronic devices. Given the special characteristics of the tests, they are usually restricted to devices containing memory blocks, where the soft error is frozen until a later reading and reporting. However, analog single event transients in discrete devices such as voltage comparators could be characterized by this tests designing appropriate code for programmable digital devices, either microprocessors or FPGAs. These devices are constantly inspecting the analog device in order to detect spurious changes in the nominal output value. Thus, the presence of transients can be detected and some information about them can be stored, the only limit being the speed of the surveying digital device.

Besides, analog comparators can be also used as an interface for other kinds of analog devices undergoing single event transients. However, this is possible only if care is taken to remove or determine the single event transient rate in the comparators that might be misled with transients in the target devices.

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