2004ESASP.536..571F

Radiation Effects on CMOS R/2R Ladder Digital-to-Analog Converters

F. J. Franco, J. Lozano and J. A. Agapito

Abstract—**The behaviour of CMOS R/2R ladder D/A converters when they are irradiated simultaneously with gamma and neutron radiation is described. The converters suffer an increase of the offset error and a reduction of the linearity because of the malfunction of the internal CMOS switches and the appearance of leakage currents. The effective inputs become "1" whatever the actual input is. No evidence of neutron damage was found.**

Index Terms—**Accelerators, CMOS technology, D/A converters, NIEL, TID.**

I. Introduction

THE cryogenic system of the LHC of CERN will require 12 bits parallel input digital-to-analog converters. These devices will be placed outside the ring that will contain the beam of heavy hadrons with a velocity about *c*. Because of the nuclear reactions, residual particles will be originated. Charged particles are supposed to stay inside the ring because of the powerful electromagnetic fields that guide the particle beam. However, the neutron and the gamma rays will be able to escape from the ring and affect the electronic instrumentation that controls the liquid helium of the refrigeration system of the superconducting electromagnets.

During ten years of the LHC lifetime, a total fluence in the order of 10^{13}-10^{14} $n{\cdot}cm^{-2}$ is expected as well as several hundreds of Gy of ionising gamma radiation [1]. The selected electronic devices must tolerate these radiation levels without risk. One of the research lines was the test of commercial CMOS converters. In this paper, the results when irradiating this kind of devices are shown.

II. The R/2R Ladder. DC Parameters of a Converter

The tested devices were AD7541A, AD7545A, DAC82222 & MX7541A converters. All these converters are based on the R/2R ladder network. Therefore, it is interesting to study its characteristics. Fig. 1 shows the basic structure of a R/2R ladder network. Using Kirchoff's laws, the following equations are deduced:

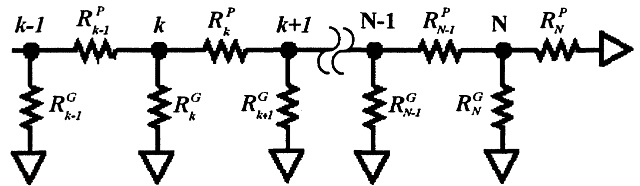

Fig. 1: Classical R/2R ladder network.

$$\frac{V_{k-1}-V_k}{R^P_{k-1}}=\frac{V_k}{R^G_k}+\frac{V_k-V_{k+1}}{R^P_k},\quad \forall k\in[2,N-1] \tag{1}$$

$$\frac{V_{N-1}-V_N}{R^P_{N-1}}=\frac{V_N}{R^G_N}+\frac{V_N}{R^P_N},\qquad if\ k=N \tag{2}$$

Usually, $V_1 = V_{REF}$, an external reference voltage. The value of the voltages at the rest of the nodes can be calculated from V_1 solving an equation system with *N* unknown variables. In case the values of the resistor are:

$$R^P_k=R,\qquad \forall k\in[1,\ N-1] \tag{3}$$

$$R^G_k=R^P_N=2{\cdot}R\qquad \forall k\in[1,\ N] \tag{4}$$

being *R* a pattern resistor, eq. (1)-(2) move into:

$$5{\cdot}V_k=2{\cdot}V_{k+1}+2{\cdot}V_{k-1},\quad \forall k\in[2,\ N-1] \tag{5}$$

$$V_{k-1}=2{\cdot}V_k,\qquad if\ k=N \tag{6}$$

The final solution of this problem must be obtained with the mathematic induction theorem and it is the following one:

$$V_1=V_{REF},\qquad V_k=\frac{1}{2}{\cdot}V_{k-1},\quad \forall k\in[2,\ N] \tag{7}$$

Therefore, the voltage at every node is half the value of the previous one and twice the value of the voltage of the following node. Moreover, the different currents that flow trough the resistor R^P_k have the same ratio. This property is very important to study the behaviour of these D/A converters.

Fig. 2 shows an electrical network based on the fig. 1 [2]. In this case, the resistors are not connected to an only ground. This node can be selected from two ones, real or virtual ground created by an operational amplifier. One way or another, previous analysis about the R/2R ladder remains being

This work was supported by the cooperation agreement K476/LHC between CERN & UCM, by the Spanish research agency CICYT (FPA2002-00912), partially supported by ITN and by the private foundation "*Miguel Casado San José*".

F. J. Franco is with the Department of Electronics, Faculty of Physics, Universidad Complutense of Madrid, Spain (e-mail: monti@fis.ucm.es).

J. Lozano was with the Department of Electronics, Faculty of Physics, Universidad Complutense of Madrid, Spain. He is now with the Sensor Laboratory, Applied Physics Institute (CSIC), Madrid, Spain (e-mail: jesloz@ifa.cetef.csic.es)

J. A. Agapito is with the Department of Electronics, Faculty of Physics, Universidad Complutense of Madrid, Spain (e-mail: agapito@fis.ucm.es).

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

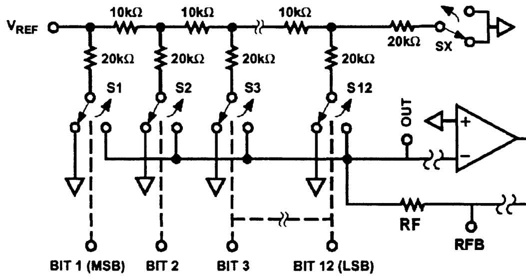

Fig. 2: R/2R network of the tested converters. The value of R is 10 kΩ so the internal resistors are 10 kΩ & 20 kΩ. The S_X switch allows to match the final R^P resistor to the R^G ones. The RF resistor is internal and similar to the R^P ones. *OUT* & *RFB* are outputs of the converters connected to an external operational amplifier.

applicable to the network. An SPDT switch controls every branch of the network.

When the switches are open, all the currents that go through R^G arrive at the real ground. However, when they are closed, the currents reach the virtual ground, are added and, finally, must be drained along the RF resistor. Thus, the sum of the currents is converted into a voltage whose value is:

$$V_O = -V_{REF}\frac{RF}{R}(S_1\cdot 2^{-1} + S_2\cdot 2^{-2} + \ldots + S_N\cdot 2^{-N}) \quad (8)$$

This value is deduced from the fact that there is a ratio of 2 between adjacent currents. S_K is the logic value of the control input and its value is either *0* or *1*. Usually, $RF = R$ and:

$$V_O = -V_{REF}\cdot(S_1\cdot 2^{-1} + S_2\cdot 2^{-2} + \ldots + S_N\cdot 2^{-N}) \quad (9)$$

The functioning of a digital-to-analog converter has just been explained. The basic unit to study the DC characteristics of a DAC is the *least significative bit* (LSB). It is defined as:

$$V_{LSB} = V_{REF} / 2^N \quad (10)$$

This unit is interesting to calculate the DAC errors that appear because of the non-idealities of the device: Leakage current through the closed switches, mismatching among the resistors, etc. So, some standard errors are defined. First, the output of an ideal converter must be 0 V if the inputs are *00..00*. However, it is not usually so and the offset error must be defined as:

$$\textit{Offset Error }(O.E.) = V_{00..0} / V_{LSB} \quad (11)$$

The origin of this errors are the leakage currents trough the switches and the offset voltage of the external operational amplifier. Also, a mathematical study of (9) allows to deduce that the output voltage for a digital input of *11..11* is:

$$V_O = \frac{2^N - 1}{2^N}\cdot V_{LSB} \quad (12)$$

Unfortunately, this relation is not usually true. The reason is the difference among the values of the internal resistors of the DAC. Therefore, a new error, called *gain error*, is defined as:

$$\textit{Gain Error }(G.E.) = (V_{11..1} - V_{00..0}) / V_{LSB} - (2^N - 1) \quad (13)$$

Finally, the mismatching of the resistors not only leads to the error gain. If the ratio between the currents inside the converter were not a power of 2, the values of V_O could not be fitted to a straight line since the values would not be an integer multiple of the LSB unit. Therefore, the ratio between the output and the input code will be non-linear and the size of the non-linearity must be estimated. The *integral non-linearity (INL)* is defined as:

$$INL(k) = [V_{OUT}(k) / V_{LSB} - O.E. - k\cdot G.E./(2^N - 1)] - k \quad (14)$$

This array is formed by the difference between the real output value, once the gain & offset errors are corrected, and the nominal one. From these values, the following parameter can be calculated:

$$N_{REL} = N - \log_2\left[|INL_{MAX}|\right] \quad (15)$$

N_{REL} is the relative number of bits of the converter. Some points should be taken into account. The relative number of bits can be very different from the real number of bits. The higher the values, the closer to ideality the converter. Only if the INL_{MAX} is higher than 1 LSB, the relative number of bits is lower than the number of inputs and the converter output does not increase with the input code and it has not got monotonic behaviour [2].

III. Design characteristics of the tested devices

The datasheets of the converters can be downloaded from the web page of each company [3]-[4]. In them, the use of thin film resistor is pointed out. Thin film resistors are built by means of the growth of a Ni-Cr alloy on a Ta-Ta_3N_5 layer above the silicon bulk. Afterwards, their dimensions are trimmed by laser [5]. This is an expansive process that is used only when the resistors tolerance must be very tight. Fig. 3 shows the results of a worst case calculus of the relative number of bits as a function of resistors tolerance. This parameter is always higher than 10 in the clean converters so a tolerance lower than 0.15% is needed to reach that accuracy.

The building of the switches that control the direction of the current is other interesting point. The core of the switch is a pair of NMOS transistors whose gate voltages are complementary. Fig. 4 shows a typical design of the switches of a D/A converter [6]. The use of two CMOS inverters can adapt the logic input to hard logic levels (ground or V_{DD}) and carry the current to the virtual or real ground.

The AD7545A & DAC8222A converters have got input data latches. The goal is to allow the activation or deactivation of the converter by means of an external control signal. So, the design is a little more complex and structures like fig. 5, extracted from the AD7545A datasheet, are integrated in the chip.

IV. Test setup

The total radiation tests were carried out at the Portuguese Research Reactor (Sacavem, Portugal). A 0.7 cm thick boron shield cut the thermal neutron component of the beam and a 4 cm thick Pb shield was used to reduce the total gamma dose

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

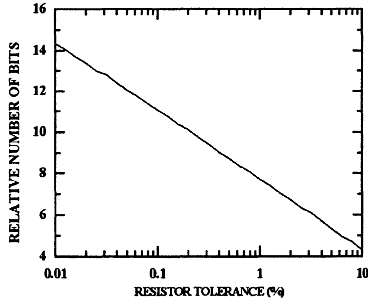

Fig.3: Relative number of bits of a D/A converter vs. the tolerance of the internal resistors. This figure was obtained from a worst case analysis of the network of fig. 2.

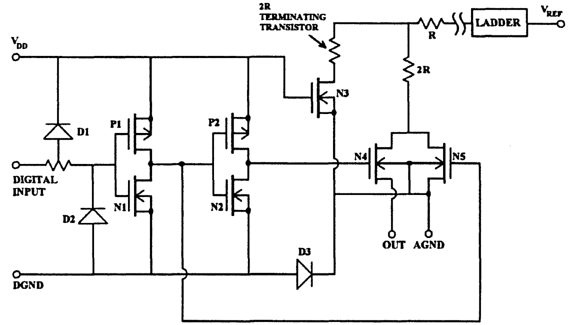

Fig. 4: Structure of an internal switch in CMOS D/A converters.

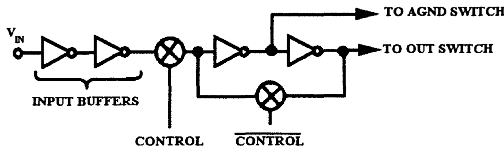

Fig. 5: Input data latches of the AD7545A converter. The control signal and its complementary one are obtained from external signals. The cross-shaped switches are NMOS transistors.

TABLE I: TOLERANCE OF THE CONVERTERS

Device	TID (Gy)	NIEL ($\cdot 10^{13}$n·cm^{-2})
AD7541AKN	565	1.20
AD7545AKN	910	1.90
MX7541AKN	325	0.68
DAC8222A	400	0.84

below 2 kGy for the centre of the cavity. The neutron energy spectrum is almost constant between 0.6-3 MeV and negligible outside these values. The neutron fission fluxes were measured with Ni detectors placed at the centre of the boxes that contained the PCBs. Photodiodes sensitive to neutrons were placed in several boards so the neutron flux was monitored online. Integration dosimeters were placed on the back of first and last PCBs and a channel for monitoring the gamma radiation was also implemented. The irradiation took place in five sessions of about 12 h followed by other stand-by 12 h.

The system used to measure the characteristics of the devices during the irradiation consisted of a personal computer, where a program developed in Testpoint was running, and some instrumentation devices: A Keithley 7002 switch system, a K2002 digital multimetre and K236 source measure unit. The PC used the standard GPIB protocol to control all the devices. Moreover, the PC has got a digital PIO12 card that was managed by the program to provide the digital 12-bit input to the converters. The PC could characterise the converters every few minutes during the irradiation. The devices were placed on test boards and they were connected to the digital multimetre and the power supplies by a low resistance & shielded 4-metre wire. The operational amplifiers (OP-27), which the converters need to work, were placed at the outside of the neutron beam. All the devices were supplied by an uninterrupted power source (UPS) to minimise the action of accidental power cuts. A detailed description of this system can be found at [7].

V. RESULTS

The converters received neutron fluence between $2.25\cdot10^{13}$ & $2.75\cdot10^{13}$ n·cm^{-2}. The vestigial gamma dose was placed between 1080 & 1300 Gy (~ 20 Gy/h). Since the CMOS devices are much more sensitive to the ionising damage than to the displacement one, the evolution of the parameters are shown as a total ionising dose (TID) function. During the irradiation, the ratio between the neutron fluence and TID was $2.1\cdot10^{13}$ n·cm^{-2} ≡ 1 kGy. Table I shows the tolerance of the converters.

Fig. 6-7 show the evolution of the offset error of the D/A converters. The offset error is stable about 1-2 LSB until a critical TID is reached. This value varied from 48 Gy on DAC8222A up to 350 Gy on AD7541A. From this value on, the offset error becomes positive if it is not so and starts growing. The limit value is 4095 LSB, which is reached when the converter destruction happens.

The behaviour of the gain error is shown in fig. 8-9. In the beginning, its absolute value is 10-20 LSB and the sign, either positive or negative. If a critical TID is reached, the error gain begins decreasing. When the destruction happens, the value is about -4095 LSB. It is important to point out to the extraordinary similarity between the gain & offset error curves on all the samples.

The relative number of bits is shown in Figs. 10-11. In most cases, it starts decreasing simultaneously to the beginning of the offset error growth. The drop is gradual except some sudden drops that happen on all the converters when the destruction is close. Only the case of AD7541A is different. First, the decrease of the relative number of bits begins earlier than the increase of the offset error. Second, there is a growth on the AD7541 converter between 425-525 Gy. It is a paradoxical but true fact that the relative number of bits of this converter decrease during the reactor stand-by time and increase while the reactor is in operation.

There is not a great increase in the device consumption. Only the logic supply V_{DD} showed a growth from 0 up to 0.5-1 µA. Neither the inputs nor the V_{REF} supply suffered a shift of the current consumption.

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

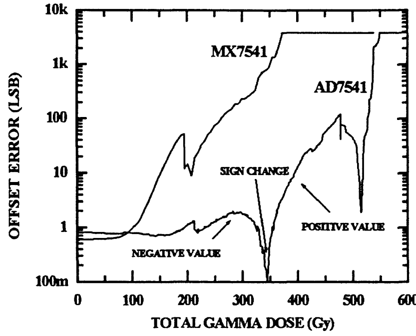

Fig. 6: Evolution of the offset error of AD7541 & MX7541 converters.

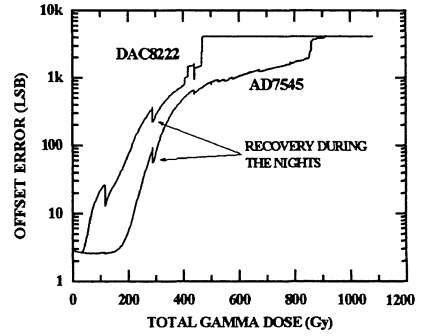

Fig. 7: Evolution of the offset error of AD7545 & DAC8222 converters.

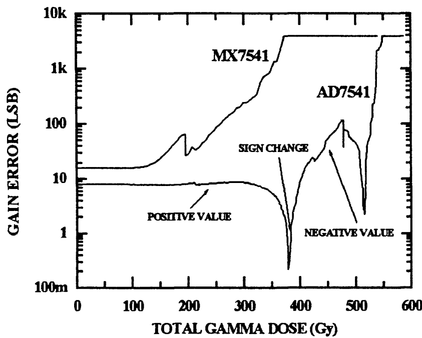

Fig. 8: Evolution of the gain error of AD7541 & MX7541 converters.

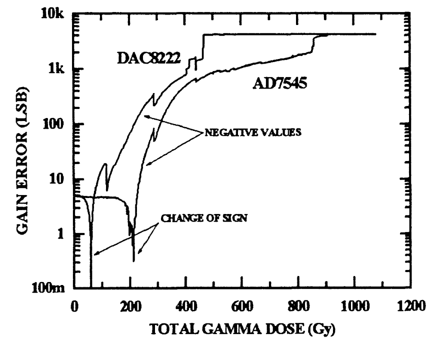

Fig. 9: Evolution of the gain error of AD7545 & DAC8222 converters.

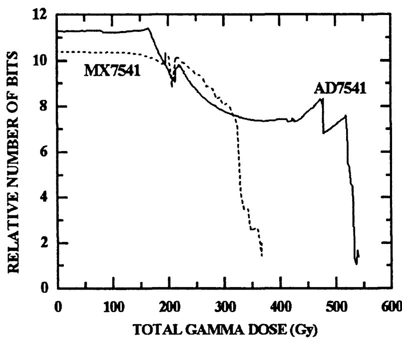

Fig. 10: The relative number of bits of AD7541 & MX7541 converters.

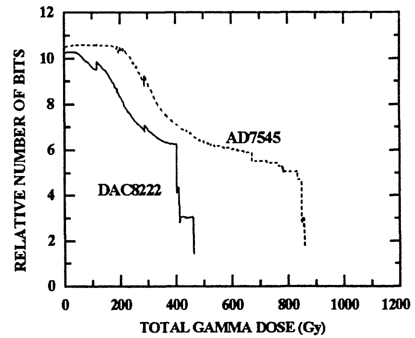

Fig. 11: The relative number of bits of the AD7545 & DAC8222A converters. The small sharp peaks of the curves are related to the annealing during the stand-by times. However, the sudden drops are caused by the destruction of some input.

VI. Discussion

The effects of the gamma radiation on CMOS devices are well known. First, a shift of the threshold voltage of the MOSFET is expected. Second, an increase of the subthreshold leakage current will appear [8]. Both phenomena can avoid a digital circuit to switch between logic states [9].

A. The malfunction of the switches as the cause of D/A converter degradation.

Fig. 12-15 show the input-output relation on the converters at some TID values. The initial shape is a straight line but, as the total ionising dose increases, the function looks like a staircase with less and less steps. Finally, it becomes a horizontal line with a value close to the reference voltage. The number of levels in the function is always related to a power of 2. This is widely explained in the figure captions. The degradation of the converters has some characteristics that allow us to find out what has happened inside them. First of all, the connection between the number of levels and the powers of 2. Also, the value of the highest input is always very close to $-V_{REF}$. Finally, the offset error remains almost constant and grows softly if a critical TID is reached.

The authors believe that the digital-to-analog converters fail because of the inability of the switches to change from virtual ground to real one. Sooner or later, the effective input will become "1". This fact explains why the output is very close to $-V_{REF}$ when the converters are very irradiated and why the input-output function shows a number of levels related to the

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

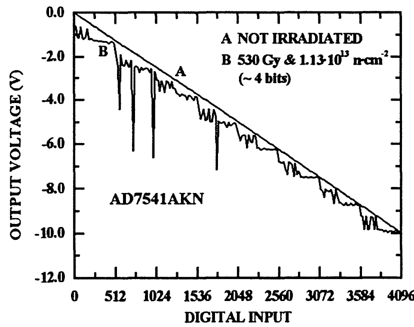

Fig. 12: Input-output relation on the AD7541A at some values of TID. Except four anomalous peaks, all the points of B are distributed in 16 values.

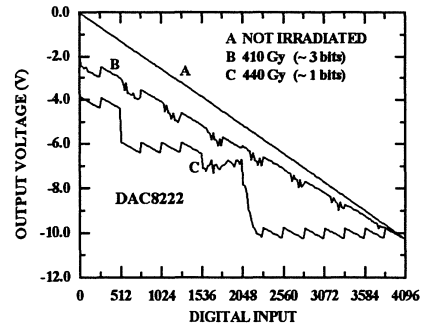

Fig. 13: Input-output relation on the DAC8222A at some values of TID. The number of peaks in each curve is a power of 2.

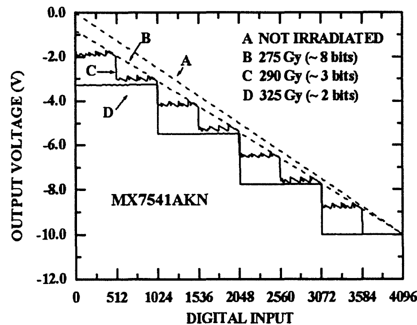

Fig. 14: : Input-output relation on the MX7541A at some values of TID. The B line goes on being a straight line but shows a very high offset error because of the switch leakage currents. The C line has eight main values. Inside each one, there are four peaks. Finally, the D line has got only four levels since only the two most significative inputs can work. The value of the output levels is not proportional because of the existence of leakage currents.

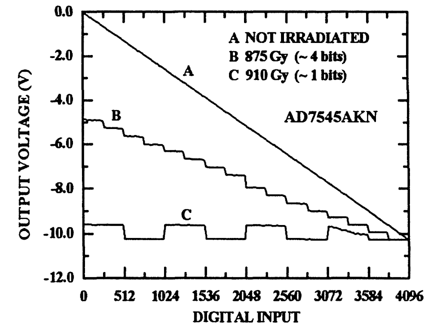

Fig. 15: Input-output relation on the AD7545A at some values of TID. There are 16 levels in the B curve. The cause is that only the second to fifth inputs can work. The other inputs are continuously closed. The C curve shows eight different intervals. The difference between them is about $V_{REF}/16$.

powers of 2. The cause might be both the diminution of the threshold voltage and the increase of the leakage current of the NMOSFET that separates the virtual ground of the operational amplifier from the R/2R ladder network. This is the N4 transistor in fig. 4.

B. Physical causes of the switches failure

There are some effects that can explain the failure of the switches. If the threshold voltage of N4 became lower than 0, it would be always ON even though the gate voltage was 0 V. So, the effect of the threshold voltage decrease is a potential cause of the disablement of the switches. Let us focus now on the influence of the subthreshold leakage currents. On the tested converters, the most significative bit is controlled by the current that flows trough the R_1^G resistor. The value of this current is 500 μA and the current that controls the twelfth bit is 4096 times lower (122 nA). The leakage current in an unirradiated transistor is very small (in the order of several pA if the gate voltage is 1 V below the threshold voltage) [10] but it increases with the total ionising dose because of the storage of positive charge in the epitaxial oxide close to the transistor [11]. The provided values by different authors [8, 11-12] are in the order of the former ones when the total ionising dose is several hundreds of Gy. Though the characteristics of the manufacturing technology are unknown, similar values can be supposed to be found at the converter transistors. In any case, the switch that blocks the path of the current to the virtual ground of the operational amplifier is not able to do it and an important current reaches the amplifier. Even if all the inputs were 0, there would be a significative current, which would lead to a negative voltage at the amplifier output. If they are large enough, which happens when the converter is very degraded, the whole of the currents flow to the virtual ground whatever the digital input is. Therefore, the output will be a flat line close to the voltage reference, as it was found in the experience.

The increase of the subthreshold current and the decrease of the threshold voltage is not sharp. So, even though the transistor have been very irradiated, their characteristics might be inside the tolerance margins so the converter could still work correctly. So, no evidence of damage could be found until some of the parameters of the transistors goes out of the tolerance margins. This explains the fact that the converters did not show any sign of degradation until a critical ionising dose was reached.

Finally, parasitic leakage currents among different NMOS transistors have been created since this fact can explain the increase of the logic supply current. However, these currents do not affect the output of the converter. If this happened, there would be a great difference between the values of $V_{I1..I}$ before and after the irradiation. This mismatch was not found.

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

C. Asymmetry in the transistors behaviour

The experience has shown enough signs that support the theory of the continuous connection of the ladder network to the virtual ground. However, this theory implies that the NMOSFET that joins the real ground to the ladder network (N5 in fig. 4) has stopped working and it does not allow the flow of current. It is something odd since it must be absolutely identical to its twin transistor, N4, because of mismatching reasons. Something breaks the symmetry of the transistors.

A possible cause is the way that the transistors are placed. Both transistors are similar but, perhaps, the parasitic channel responsible of the N4 subthreshold is easier to be created than N5 one.

Other chance is the fact that the logic input stage could be damaged. If the logic levels of the output connected to N5 were different to N4 one, the behaviours of both transistor would not be similar. Last hypothesis is possible but hard to believe. It is strange that it does not depend on the existence of input data latches. Moreover, even though there were a great difference between the logic outputs, a leakage current through N5 had to be observed but it was not.

In short, the authors believe that the first hypothesis is correct. It does not depend on the logic stage but in the placement of the transistors. However, a full knowledge of the internal structure is needed to find out the reason of the inability of the N5 transistor.

D. Evolution of converter errors

In the beginning, the offset error is directly related to the input offset voltage of the operational amplifier and, to a lesser extent, to the bias current of the opamp inverting input and to the converter leakage currents. Also, the data are taken by means of a system that is not free of errors: E. g., the converter is 5 m away from the operational amplifier. Thus, an offset error of several LSB was observed in the converters since the measuring system started to run until the irradiation began.

These error sources were systematic so the offset value keeps constant and hardly moves from the original one until the converter is damaged enough. Positive charges are accumulating step by step inside the epitaxial oxide but the leakage currents cannot appear immediately. A minimum concentration of charges is needed to attract enough electrons and build the parasitic channels. Therefore, the offset error hardly changes during the first stage of the irradiation (Fig. 6-7).

Once the number of charges is high enough, the leakage currents appear. If all the logic inputs are 0, the leakage currents converge at the virtual ground of the operational amplifier and set a non-zero voltage at the opamp output due to RF. This is the cause of the offset growth measured during this experience. The offset error grows in proportion to the leakage currents of the converter and reaches 4095 LSB when they are large enough to absorb the whole of the R/2R network currents.

Other interesting fact is the similarity between the gain & offset error in all the D/A converters when the total ionising dose is high enough (Fig. 6-9). The only difference is the sign. It can be easily explained from the characteristics of the evolution of the converters. The output value with all the inputs equal to "1" does not change during the irradiation since all the switches become closed. An alternative expression of (4) is:

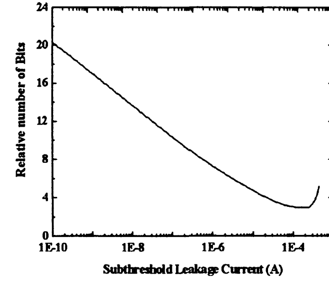

Fig. 16: Relative number of bits vs. subthreshold leakage current. All the switches were supposed similar and the subthreshold current is the same in all the switches. The resistors were exactly 10 kΩ and 20 kΩ, being the tolerance of 0%.

$$G.E. = [V_{11..1} / V_{LSB} - (2^N - 1)] - O.E. \quad (16)$$

The value of $V_{11..1}$ hardly changes during the irradiation. Moreover, the first values of the offset error are about 0 LSB. Therefore:

$$G.E. \cong G.E._{TID=0} - O.E. \quad (17)$$

$G.E._{TID=0}$ is the initial value of the gain error. Its value is not higher than 10-15 LSB and, as the irradiation is carried out, $O.E. >> G.E._0$, thus, the gain error follows the offset error:

$$G.E. \cong -O.E. \quad (18)$$

The reduction of the relative number of bits is related to several things. First, to the direct removal of active switches because of the radiation. The lower the significance of the bits, the larger the action of the leakage current. Therefore, the least significative bits will fail quickly because of the leakage currents trough the switch. In both cases, the switch would not be able to work and the effect would be the direct loose of bits. Moreover, even though all the switches work, the leakage currents make false eq. (1)-(2) since an additional element must be inserted. So, the D/A converters stop being linear and the relative number of bits decreases.

Fig. 16 is a calculus of this parameter as a function of the subthreshold leakage currents. Even though the resistors are completely matched in the simulation, if the subthreshold leakage current is higher than 32 nA, the relative number of bits is lower than 12. Curiously, the relative number of bits increases if the leakage currents are large enough. The cause is simple: When these currents are too important, the converter shows only one output value ($-V_{REF}$). Nevertheless the converter is destroyed, the output function is a flat and straight line so the INL, which is a method to measure the converter linearity, is 0 whatever the digital input is. On the other hand, in this case the offset error is 4095 LSB and the gain error –4095 LSB.

Naturally, if the growth of the offset error and the decrease of the relative number of bits are related to the leakage currents, they both must appear simultaneously. This fact is observed on most converters. However, in the case of the AD7541A, the relative number of bits starts decreasing much

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

earlier than the growth of the offset error (fig. 8, 10). A quick look at fig. 12 allows us to identify the origin of the loss of accuracy. Almost every input code of this converter has got an output voltage close to the theoretical one, very few input codes (567, 735, 987 & 1722) have got output values far from the theoretical value. However, these few codes have a very high INL so the highest value of this parameter is large. Therefore, the relative number of bits will be low although most of the input codes show the theoretical value and only three or four codes show an actual value very different from it. As the irradiation goes on, the strange responses of the codes are not noticed any more and the relative number of bits increases, just as fig. 10 shows. The authors cannot give any satisfactory explanation of the odd behaviour of this converter.

E. *Influence of displacement damage on the converters*

So far, the discussion has been about the action of total ionising dose on the converters although the converters had been irradiated with neutrons, too. However, the authors believe that their influence is negligible. The displacement damage affects specially the lifetime of minority carriers and the majority carrier concentration and mobility in semiconductors [13]. The internal resistors of these converters are built in thin film technology so they are not semiconductors but metals. Metals are high radiation tolerant [14] so no shift at the value of the resistors is expected.

The only weak points are the transistors that form the analog channels of the switch. Because of the diminution of carrier mobility, an increase of the parasitic resistor might happen but it is likely that it would be less important. This statement is based on three reasons: First of all, the carrier removal and the mobility growth is only important at much larger neutron fluences than that received by the converters ($\sim10^{15}$-10^{16} n·cm^{-2}) [15]. Second, the parasitic resistance increase could be compensated by the diminution of the threshold voltage of the NMOSFET. According to [16], the resistance of an analog switch can be calculated as:

$$R_{SW} = \frac{1}{\beta \cdot (V_{GS} - V_T)} + R_{PAR} \quad (19)$$

β is the trasconductance of the NMOS transistor, V_{GS} & V_T the gate-to-source and threshold voltages and R_{PAR} the parasitic resistance of the transistor. Though β gets lower and R_{PAR} higher because of the displacement damage and drives the switch resistor higher, V_T decreases according to the ionising dose and the effect is the complementary. It could make R_{SW} decrease. Therefore, both effects could overlay each other and the value of the resistance would not shift too much.

Any case, the switches are designed to have the lower possible resistance since they are less reproducible than the expensive thin film resistors. Therefore, although the parasitic resistances can grow, they are negligible.

However, it is not true that the entire CMOS R/2R ladder D/A converters are neutron radiation tolerant. The neutron tolerance of high accuracy converters is due to the use of metallic resistor. The use of this kind of resistor is expensive so diffusion resistors are usually found in converters with a lower number of bits [5]. These resistors can suffer not only the effects of the carrier removal or the mobility reduction but the action of the reduction of minority carrier lifetime. The resistors are built by means of diffusing acceptor impurities inside an *n* substrate. So, a parasitic PN junction is build and it must be reverse biased. It is well known the fact that the leakage current in reverse biased PN junction increases with neutron radiation because of the increase of generation-recombination currents [15], which are directly related to the value of the average minority carrier lifetime [17]. These leakage currents could be large enough to affect the behaviour of the D/A converter. Unlike the leakage currents that were found in the NMOS switches, these ones take place all over the resistor surface and go to the substrate. A study has shown that these currents can increase greatly the non-linearity of the converters [18]. Definitively, the results shown in this paper should not be extended to low accuracy converters.

VII. Conclusion

The CMOS R/2R ladder converters under gamma radiation suffer an increase of the offset error because of the appearance of subthreshold leakage currents and the failure of the switches. This leads also to linearity losses that cause the increase of the INL and the reduction of the relative number of bits. The malfunction of switches was observed and registered by the PC controlled measure system. This behaviour is independent on the existence of internal latches in the input stage. The action of the neutron radiation on these devices was negligible compared to the ionisation damage.

Other works has been carried out to evaluate the behaviour of the D/A converters under ionising radiation, i.e. [19, 20]. In these works, the authors tested 12 input D/A converters under gamma radiation. Their results are quite similar as the ones we report in this paper.

References

[1] The LHC Study Group, *"The Large Hadron Collider. Conceptual Design"*, CERN/AC/95-05(LHC), CERN Desktop Publishing Service, 1995.

[2] D. A. Johns and K. Martin, *"Analog Integrated Circuit Design"*, John Willey, 1997.

[3] Analog Devices Inc. *http://www.analog.com.*

[4] Maxim Integrated Products *http://www.maxim-ic.com.*

[5] W. K. Chen, "The VLSI Handbook", CRC Press LLC, USA, 2000.

[6] M. Alexander, "Understanding and preventing latch-up in CMOS DACs", *App. Note AN-109, Analog Devices.*

[7] J. Lozano , F.J. Franco, J.A. Agapito, J.P. Santos "Instrumentation system for test of electronic components subjected to neutron radiation", *proceedings of SAAEI 2002*, September, 18th -20th, Alcalá de Henares, (SPAIN).

[8] J. R. Srour and J. M. McGarrity, "Radiation Effects on Microelectronics in Space", *Proceedings of the IEEE, vol. 76, iss.11, pp. 1443-1469, November 1988.*

[9] S. E. Kerns and B. D. Shafer, "The Design of Radiation-Hardened ICs for Space: A Compendium of Approaches", *Proceedings of the IEEE, Vol. 76, no. 11, pp. 1470-1509, November 1988.*

[10] S. M. Sze, *"Physics of Semiconductor Devices"*, Second Edition, John Wiley & Sons, Inc. U.S.A, 1981.

[11] O. Flament, C. Chabrerie, V. Ferlet-Cavrois and J. L. Leray, "A methodology to study lateral parasitic transistors in CMOS technologies", *IEEE Transactions on Nuclear Science, vol. 45, iss. 3, pp. 1385-1389, June 1998.*

© European Space Agency • Provided by the NASA Astrophysics Data System

2004ESASP.536..571F

[12] H. Kamimura, M. Sakagami, S. Uchida, and M. Kato, "Total-dose hardness assurance-testing for CMOS devices in space environment", *Proceedings of Reliability and Maintainability Symposium, Las Vegas (USA), January 21-23, 1992*

[13] G. C. Messenger, "A summary review of the displacemente damage from high energy radiation in silicon semiconductors and semiconductor devices", *IEEE Transactions on Nuclear Science, vol. 39, iss. 3, pp. 468-473, June 1992*

[14] J. R. Srour and J. M. McGarrity "Radiation Effects on Microelectronics in Space", *Proceedings of the IEEE, Vol.76, Iss. 11, pp.1443-1469, November 1988.*

[15] G C. Messenger and M. S. Ash, "*The Effects of Radiation on Electronic Systems*" , 2nd. Edition, New York, Van Nostrand Reinhold, 1992.

[16] P. Horowitz and W. Hill, "The Art of Electronics", 2nd Edition, Cambridge University Press, USA, 1989.

[17] M. S. Tyagi, "*Introduction to Semiconductor Materials and Devices*", John Wiley & Sons, Inc, Singapore, 1991

[18] P. C. Maulik, "Analysis of leakage current induced nonlinearity in resistor-ladder based data converters", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 47, no. 2, pp. 136-137, February 2000.*

[19] A.K. Sharma, K. Sahu, and S. Brashears, "Total ionizing dose (TID) evaluation results of low dose rate testing for NASA programs", *IEEE Radiation Effects Data Workshop, 1996., pp.13-18.*

[20] M. V. O'Brian et alt. "Radiation damage and single event effect results for candidate spacecraft electronics", *IEEE Radiation Effects Data Workshop, 2000., pp. 106-122.*

© European Space Agency • Provided by the NASA Astrophysics Data System