Growth and Interface Engineering of Highly Strained Low Bandgap Group IV Semiconductors

S. Wirths[1*], M.A. Pampillón[1,2], E. San Andrés[2], D. Stange[1], A. T. Tiedemann[1], G. Mussler[1], A. Fox[1], U. Breuer[3], J-M. Hartmann[4], S. Mantl[1] and D. Buca[1]

[1]*Peter Grünberg Institute (PGI 9) and JARA-FIT, Forschungszentrum Juelich, 52425, Germany,*
[2]*Dept. Fis. Aplic. III: Electr. y Electron., Univ. Complutense de Madrid (UCM), Madrid, 28040, Spain*
[3]*Central Division of Analytical Chemistry (ZCH), Forschungszentrum Juelich, 52425, Germany*
[4] *CEA, LETI, Minatec Campus, 17 rue des Martyrs, 38054 Grenoble, France*

[*]*Tel: +49 2461-61-3149, Fax: +49 2461-61-4673, E-mail: s.wirths@fz-juelich.de*

1. Introduction

To further improve the performance and power consumption of integrated circuits (IC) alternative channel materials to Silicon (Si) as well as novel device concepts attract more and more research interest. Especially, Germanium (Ge) is a promising candidate for several reasons. First, Ge offers the highest bulk hole mobility of any known semiconductor material [1] promising high p-MOSFET performances in terms of drive currents. On the other hand, due to its low and quasi-direct bandgap, Ge is also used for low power devices such as Tunnel-FETs [2]. These properties might be even enhanced by strain engineering or alloying Ge with Sn [3,4]. However, introducing high biaxial tensile strain in Ge or GeSn remains a challenge because of missing adequate buffer technology. High quality CVD epitaxy of GeSn layers enables a new degree of freedom in Ge(Sn) strain engineering.
In this contribution, we will present the epitaxial growth of highly tensely strained Ge and GeSn layers up to 1.4 % and 0.4 %, respectively, using high Sn-content (Si)GeSn buffer layers. In this context, electronic band structure calculations including effective masses at certain points in the Brillouin zone will be provided. In Fig. 1 the bandgap narrowing induced by strain is highlighted. Applying 1.4 % tensile strain results in a bandgap reduction of 162 meV and an energy difference between Γ- and L-valley of solely 14 meV. Via MOS-capacitors (MOSCAPs) the surface passivation as well as interface quality of the low bandgap materials is addressed. In this context, the CMOS process limitations towards integration concerning strain preservation and Sn segregation are discussed.

2. Experimental

(Si)GeSn buffer layers on Ge virtual substrates (Ge-VS) were epitaxially grown by Reduced-Pressure CVD (RP-CVD). Ge(Sn) layers grown on high Sn

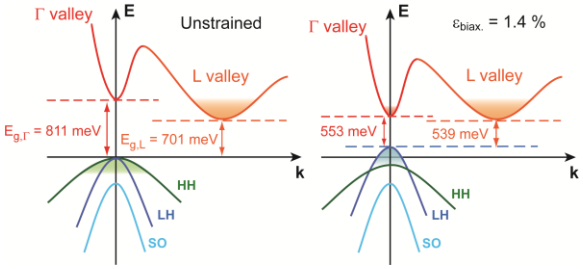

Fig. 1. Sketch of the electronic bandstructure of unstrained and 1.4% biaxial tensile strained Ge.

content strain relaxed GeSn buffers exhibit high biaxial tensile strain determined by X-Ray Diffraction Reciprocal Space Maps (XRD-RSM). In order to investigate the crystalline quality Transmission Electron Microscopy (TEM) and Rutherford Backscattering Spectrometry (RBS) were employed. For the gate stack formation HF:HCl cleaned samples were loaded into an Atomic Layer Deposition (ALD) reactor. 1 nm Al_2O_3 deposition was followed by *in-situ* O_3 oxidation and 4 nm Al_2O_3 or HfO_2. Ex-situ metallization (50 nm Pt) defines the MOSCAP structures and 10 minutes Forming Gas Annealing (FGA) completes the fabrication process. Here, devices annealed at different temperatures between 300 – 400°C were analyzed by Time-of-Flight Secondary Ion Mass Spectroscopy (ToF-SIMS) and XRD-RSM regarding strain preservation and Sn segregation. The following electrical characterization by means of temperature dependent (300 K – 77 K) Capacitance - Voltage (C-V) measurements provides information about the interfacial layer quality.

3. Results and Discussion

In order to tensely strain Ge we employ lattice engineered GeSn buffers with large in-plane lattice constants. Here, high Sn content can be achieved due to low growth temperatures 350°C and high growth

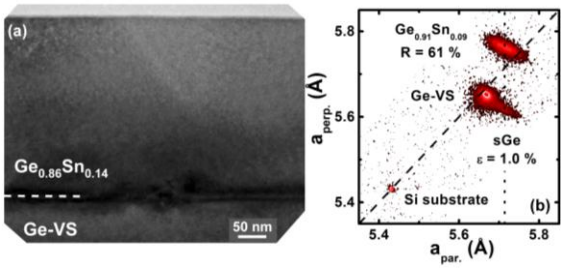

Fig. 2. (a) TEM Micrograph of a strain relaxed $Ge_{0.86}Sn_{0.14}$ buffer layer. (b) XRD-RSM of a biaxially tensile strained Ge layer (ε = 1 %) grown on a $Ge_{0.91}Sn_{0.09}$ buffer.

rates at the same time. In Fig. 2a a TEM micrograph of 250 nm $Ge_{0.86}Sn_{0.14}$ is shown. This layer thickness exceeds the critical thickness for strain relaxation by far resulting in plastic strain relaxation. Hence, a high density of misfit dislocations was observed at the GeSn/Ge-VS interface but no dislocations, e.g. threading dislocations, were found in the top part of the layer. With this technique strained Ge layers with thicknesses up to 70 nm and maximum strain of 1.4% were fabricated.

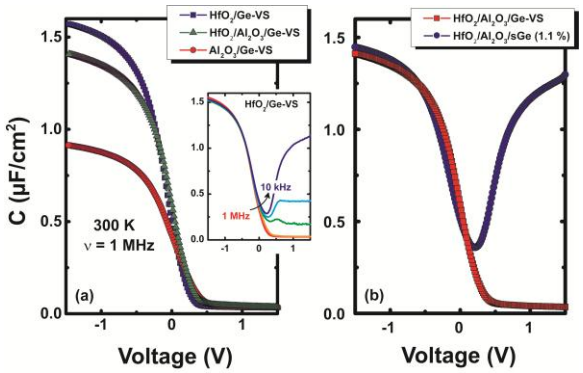

Fig. 3. Room temperature CV measurements after 300°C FGA at 1 MHz for (a) three different gate stacks on Ge-VS and (b) $Pt/HfO_2/Al_2O_3$ stacks on Ge-VS and sGe.

Exemplary, XRD-RSM data of a strained Ge/GeSn/Ge-VS structure are presented in Fig. 2b. Here, a $Ge_{0.91}Sn_{0.09}$ buffer layer with a degree of strain relaxation of 61 % was employed and a strain level of about 1 % was measured in the Ge top layer. A crucial step towards device integration of these highly strained materials is the gate stack formation. In Fig. 3a C-V measurements of three different kinds of gate stacks upon Ge-VS are presented. Steep CV-curves without D_{it} humps were found for all investigated gate stacks including $Pt/HfO_2/Ge$, $Pt/HfO_2/Al_2O_3/Ge$ and $Pt/Al_2O_3/Ge$. The highest capacitance in accumulation is obtained for 5 nm HfO_2 and offers an Equivalent Oxide Thickness (EOT) of about 1.8 nm. Using sGe (Fig. 3b) a very high inversion response even at 1 MHz was observed. Due to the much lower bandgap, minority carriers got activated leading to a high minority response in inversion. Low temperature measurements were performed to reduce the effect of minority carriers, see Fig. 4. As can be seen for strain levels of about 1.1 % nearly no inversion response was observed, whereas at the highest investigated tensile strain of 1.4 %, the lowest bandgap of about 540 meV (see Fig. 1), the inversion response could not be frozen out. For Ge MOSCAPs a D_{it} determination of about $2\text{-}5x10^{12}$ $cm^{-2}eV^{-1}$ was extracted. However the large influence of the minority carriers makes the D_{it} extraction based on the conductance method challenging.

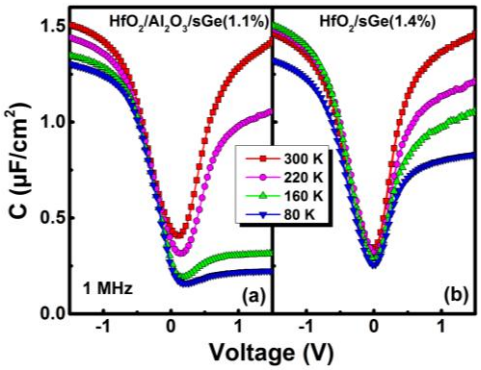

Fig. 4. CV measurements for (a) $Pt/HfO_2/Al_2O_3/sGe$ (ε = 1.1 %) and (b) Pt/HfO2/sGe (ε = 1.4 %) gate stacks at temperatures between 80 K and 300 K.

4. Conclusions

Highly tensile strained Ge(Sn) layers epitaxially grown on GeSn strain relaxed buffer layer have been presented. Electrical characterization exhibits good interfacial quality of the high-k gate stacks employing HfO_2 on Ge and strained Ge. These results mark a first step towards electronic device integration of low bandgap highly tensely strained group IV semiconductors.

References

[1] R. Pillarisetty, Nature 479 (2011) 324.
[2] G. Han, P. Guo, Y. Yang, C. Zhan, Q. Zhou, Y.-C. Yeo, Appl. Phys. Lett. 98 (2011) 153502.
[3] M. V. Fischetti, S.E. Laux, J. Appl. Phys. 80 (1996) 2234.
[4] S. Wirths, A.T. Tiedemann, Z. Ikonic, P. Harrison, B. Holländer, T. Stoica, G. Mussler, M. Myronov, J.M. Hartmann, D. Grützmacher, D. Buca, S. Mantl, Appl. Phys. Lett. 102 (2013) 192103.