

SEU Characterization of Three Successive Generations of COTS SRAMs at Ultralow Bias Voltage to 14.2 MeV Neutrons

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Abstract—This paper presents a SEU sensitivity characterization at ultra-low bias voltage of three generations of COTS SRAMs manufactured in 130 nm, 90 nm and 65 nm CMOS processes. For this purpose, radiation tests with 14.2 MeV neutrons were performed for SRAM power supplies ranging from 0.5 V to 3.15 V. The experimental results yielded clear evidences of the SEU sensitivity increase at very low bias voltages. These results have been cross-checked with predictions issued from the modeling tool *MULTI-SCALES Single Event Phenomena Predictive Platform* (MUSCA-SEP³). Large-scale SELs and SEFIs, observed in the 90-nm and 130-nm SRAMs respectively, are also presented and discussed.

Index Terms—COTS, SRAM, neutron tests, radiation hardness, reliability, soft error, low-bias voltage

I. INTRODUCTION

COMMERCIAL Off-The-Shelf (COTS) CMOS Static Random Access Memories (SRAMs) have recently arisen as an interesting alternative to space-qualified SRAMs, which opens promising perspectives to democratize fields such as avionics and aerospace. The reasons are their affordable cost and that most modern devices implement error detection and corrections mechanisms. For instance, the well-known Error Correcting Codes (ECCs) make modern SRAMs very reliable to Single Event Effects (SEEs).

In such fields, not only is reliability a major concern, but also keeping the required energy consumption constraints,

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which is critical in autonomous systems. Dynamic Voltage Scaling (DVS) is an interesting technique that consists in increasing or decreasing the bias voltage of certain components of microelectronic devices [1] depending upon circumstances. It can help to attain this objective since the switching energy has a square dependence on the supply voltage [2]. In addition, although SRAMs are volatile memories, it has been reported that they can be kept idle at very low bias voltages without losing information [3].

However, it is also a well-known issue that, as the bias voltage lowers, the critical charge needed to modify the information of a memory cell decreases as well [4], [5]. Consequently, in harsh environments, where the impact of a high-energy particle can provoke a so-called Single Event Upset (SEU), the sensitivity of these devices needs to be specifically studied. Some studies in the literature have presented experimental evidences of said voltage scaling effects, for different manufacturing materials [6] and even for academic custom D Flip-Flops [7] and SRAM cells [8]. However, little work was carried out in COTS devices. In [9] and [10], the authors studied the sensitivity of COTS Advanced Low Power SRAMs (A-LPSRAMs) and CMOS SRAMs, manufactured in 150-nm and 90-nm technologies respectively, at 0.5 V - 3.3 V.

This paper presents an experimental study of the sensitivity against 14 MeV neutrons of three successive generations of COTS SRAMs, manufactured by Cypress Semiconductor in 130, 90 and 65-nm CMOS processes, when powered up at bias voltages ranging from 0.5 V to 3.15 V. The sensitivity trends of these SRAMs for this range of bias voltages are presented and discussed. In addition, the Multiple Cell Upsets (MCUs), which are multiple errors provoked by the impact of a single particle, were extracted by using proprietary information provided by the manufacturer. Accurate cross sections for events with different multiplicities are presented as well. This point is especially relevant since newer technologies are increasingly more sensitive to MCUs [11]. The appearance of other events, such as micro Single Event Latchups (micro-SELs), occurring extremely often in the 90-nm memory, is also discussed.

In a previous work [10], the authors presented a sensitivity characterization of the same 90-nm memory as the one presented in this paper. Unfortunately, the experimental characterization was not complete due to a latchup occurred at 1.4 V and due to technical and safety reasons. In that work, the experimental data were completed with results obtained

in another previous experiment at nominal voltage on other sample from another batch. Quite high disagreements in the sensitivities of both samples were observed in that work, which were attributed to the fact of comparing samples from two different batches, and to the typical margin errors of the experimental setup of the facility. Therefore, in order to have more accurate and consistent data, in this experiment another sample of this SRAM was examined again under radiation with the same experimental setup as the two other 130-nm and 65-nm ones.

II. EXPERIMENTAL SETUP

The tests were carried out in May 2017 on three generations of Cypress Semiconductor COTS SRAMs with a capacity of 16 Mbits and configured as $2M \times 8$ bits. The tested samples are summarized in Table I, which also presents the bias voltages at which each one of them were tested.

According to the manufacturer, the nominal bias voltage of these memories ranges from 2.7 V to 3.6 V. Thus, an average value between these two values (3.15 V) was used as nominal voltage supply. It was experimentally verified that the memories were fully operational even at 1.9 V. Below this value, the readout system did not work but they still retained information. In fact, it was also verified that, for all the bias voltages in the ranges of Table I, in an environment without radiation, the information previously written in the memories was not lost.

The 130-nm and 90-nm SRAMs do not implement any error correction and detection mechanism, but a bitcell interleaving that prevents the occurrence of multiple events within the a single word provoked by the impact of the same particle. On the contrary, the 65-nm SRAM implements an ECC mechanism that corrects single errors and detects multiple ones in a single word. The latter was examined by keeping this feature active (configuration by default) and by deactivating it using a proprietary information provided by Cypress. Thus, it was possible to observe the sensitivity against neutrons of this SRAM at the technological level. The efficiency of said ECC was also assessed, and the results are discussed in Section IV-C.

Static tests were carried out: the memories were initially written with the *checkerboard* pattern (0×55), then they were radiated in rounds ranging from 1 to 5 minutes each, and examined afterwards. Tests were performed at the GENEPI2 (*GE*nérateur à *NE*utrons *P*ulsés *I*ntenses) neutron facility, which is located at the LPSC (Laboratoire de Physique Subatomique et Cosmologie) in Grenoble, France [12]. Neutrons were produced with an average energy of 14.2 MeV at fluxes that ranged from 2.00×10^7 to 2.41×10^7 $n \cdot cm^{-2} \cdot s^{-1}$. Each round of reading had its particular flux and exposure time and these data are taken into account in the analysis presented in the next sections. In any case, the target memories were always placed 32 mm away from the neutron source.

The test system comprised a motherboard with a PIC18F85J90 microcontroller, which runs the test software. An extension board with a TSOP48 socket for the SRAM under test was attached to it. All the tested SRAMs were

Table I
TESTED MEMORIES AND OPERATIONAL BIAS VOLTAGES

Memory	Technology process	V_{CC} range
CY62167DV30LL 55ZXI	130 nm	0.7V – 3.15V
CY62167EV30LL 45ZXI	90 nm	0.5V – 3.15V
CY62167GE30-4 5ZXI	65 nm	0.8V – 3.15V

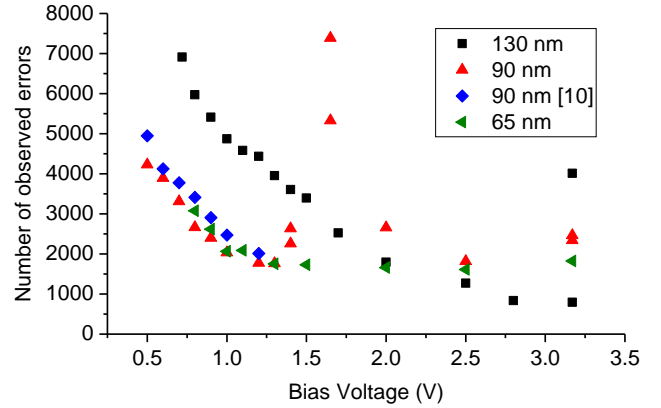


Figure 1. Number of errors observed in the studied SRAMs, for different voltage levels.

pin-to-pin compatible, hence switching from one sample to other one was extremely easy. Both the microcontroller and the SRAM were biased by two independent power supplies, which made possible to tune that of the SRAM from 0 to 3.15V. More details about the test infrastructure can be found in [9] and [10].

III. EXPERIMENTAL RESULTS

First of all, the raw number of errors observed for different voltage supplies is presented in Figure 1. In order to perform fair comparisons, the data depicted in this figure were scaled linearly to a fluence of 2.75×10^9 $n \cdot cm^{-2}$. It is important to note that not all the reading rounds were performed after exposing the SRAM to the same neutron fluence. The reason is that, for a given DUT position, the neutron flux generated at GENEPI2 can vary in a range of $\pm 10\%$ from a run to another due to the variation of beam current on the neutron production target. The objective of this figure is to provide a general idea of the behavior under radiation of these SRAMs to a potential user, whereas a finer analysis of these errors will be made in Section IV.

In the figure, it can be observed that the sensitivity trend of the 130-nm and 65-nm samples is very clear. On the one hand, the errors observed in the 130-nm SRAM increase as the voltage scales down, and the curve gets steeper for ultra-low bias voltages. In fact, at 0.8 V the number of events is 8.5 times higher than at 3.15 V. On the other hand, the sensitivity of the 65-nm sample is higher than that of the 130-nm one at nominal voltage, but on the contrary, it barely increases below that level. Only at 1.2 V, the curve starts to get steep, but at the worse case (0.8 V) it does not even double the value obtained at 3.15 V.

Figure 1 also shows a disagreement for the 130-nm SRAM at 3.15 V: curiously, after the very first reading round carried out with this memory after 5 minutes of irradiation, a micro-SEL was observed. It was easily identified due to a clear reduction in the voltage level (from 3.15 V to 2.9 V) and the fact that successive reading rounds yielded errors that were not corrected after writing the correct data on the affected memory positions. This situation could only be fixed by turning off and on again the voltage supply and that was the reason why subsequent reading rounds were limited to 3 minutes instead of 5 minutes. No micro-SEs were observed on this sample subsequently.

Finally, two sets of data are depicted for the 90-nm SRAM: the data obtained in [10] (shown here again as reference) and the new data regarding the more recent experiments. Both sets of data seem to be quite consistent even though the tested samples did not belong to the same batch. However, the new data exhibits a different phenomenon: the existence of unexpected and unpredictable highs and lows above 1.3 V. In all the cases, they were attributed to micro-SEs. The exposure times ranged from 5 minutes to only 1 minute, and in all the cases except at 2.5 V, the CY62167EV30LL sample exhibited that behavior. The observed phenomena are not consistent with the typical damage caused by dose cumulation, since the very first run at 3.15 V on this sample already yielded a micro-SEL. However, for further runs at ultra-low bias voltages (lower than 1.40 V), this kind of errors was no longer observed. The reason is that the parts are regulated, and below a certain voltage, the regulator collapses. Hence it will be difficult to latch anymore. Thus, there is no reason to think that this SRAM is specially robust against this phenomena at 2.5 V. Instead, the fact that no micro-SEL was observed at that bias voltage seems purely fortuitous.

The previously depicted phenomena is consistent with the behavior observed by Tsigiliannis et al. [14], [15], where large-scale MCUs were found and analyzed. In fact, this extreme sensitivity of 90-nm Cypress SRAMs is well known from quite a long time ago [16]. It is interesting to observe that this problem was a major issue in this technology, but it was apparently solved in the subsequent one (65-nm).

IV. DISCUSSION

It is clear that the data depicted in Figure 1 "as is" cannot be used to extract conclusions about the sensitivity of the tested SRAMs. The reason is that, in the same plot, many types of events are not distinguished: Single Bit Upsets (SBUs), where one particle affects only one memory cell; Multiple Cell Upsets (MCUs), where the same particle affects simultaneously several adjacent memory cells belonging to different words; Multiple Bit Upsets (MBUs), where several bits in the same word are affected; and even micro-SEs. This section makes a deeper analysis of these types of events separately.

A. SBU/MCU Sensitivity

Figure 2 shows the SBU/MCU cross sections of the three tested samples, once the MCUs were extracted from the set of observed SEUs. For this purpose, proprietary unscrambling

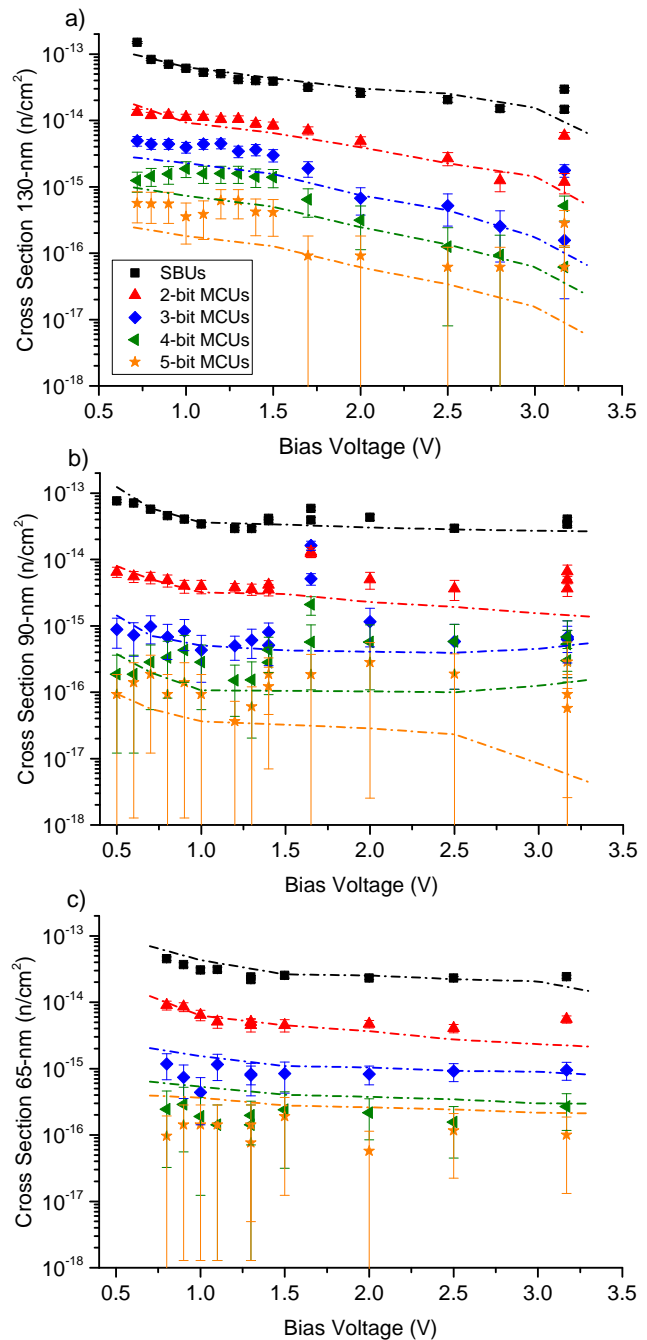


Figure 2. Cross sections of a) 130-nm, b) 90-nm and c) 65-nm SRAMs tested under different bias voltage levels. Dashed lines correspond to predictions issued from MUSCA-SEP³ [13].

information provided by Cypress Semiconductor was used for the three SRAMs. In all the cases, MCU cross sections are classified by multiplicity. Error bars have been obtained with a 95% confidence as explained in [17] (from SBUs to 5-bit MCUs). Dots in Figure 2 represent experimental data, whereas dashed lines correspond to predictions issued from the MUSCA-SEP³ modeling approach.

By checking the experimental data of the three plots, it can be observed that the SBU/MCU sensitivity significantly increases at very low voltages, especially at near-threshold ones. This is especially clear for the 130-nm and the 65-nm

Table II
EXPERIMENTAL ROUNDS WHERE LARGE MCUS (>5-BIT) WERE OBSERVED. FOR SIMPLICITY, THE ROUNDS WHERE SUCH LARGE MCUS WERE NOT OBSERVED ARE NOT DISPLAYED

SRAM	VCC (V)	6-bit	7-bit	8-bit	9-bit	≥ 10 -bit
130 nm	0.70	1	5	0	1	0
	0.80	4	0	1	0	0
	0.90	6	0	1	0	0
	1.00	2	1	1	1	1
	1.10	6	0	1	0	2
	1.20	5	1	1	0	0
	1.30	7	1	2	1	1
	1.40	3	2	1	0	0
	1.50	3	0	0	0	0
90 nm	0.60	0	0	0	1	0
	0.70	1	0	0	0	0
	1.00	0	1	0	0	0
65 nm	1.10	0	1	0	0	0
	1.30	1	0	1	2	1
	2.00	0	0	0	1	0
	2.50	2	1	0	0	0
	3.15	1	1	0	0	0

SRAMs. However, for the 90-nm one, the existence of microSELs above 1.4V makes more difficult to reach conclusions at near-nominal voltage levels. The charts display all the rounds of reading that were made (in some cases, several rounds were carried out at the same VCC). The experimental data observed for the 90-nm SRAM is consistent with the results presented by Pawlowski et al. [18], where it can be observed that the sensitivity for all types of MCUs barely increased in the range of 0.3V-1.0V. It is also consistent with the results obtained in 2015 in another sample of the same memory, presented in our previous work [10].

The figure also shows that the MUSCA-SEP³ predictions match the experimental data in a very accurate way. Even those of ≥ 5 bit MCUs accurately match the experimental data although, as mentioned above, they are not displayed in Figure 2 for practical reasons. A few small disagreements can also be observed; for instance, for the 2-bit MCUs in the 65-nm SRAM. The origins of these disagreements are multiple and can be attributed to limitations of modeling, such as topologies (elementary cell design, distance between adjacent cells, symmetry rules), back-end descriptions (mainly thickness) or bias voltage impact on the transport model.

A few MCUs with multiplicity ≥ 6 were also observed, but the error margins of the experimental cross sections were so high that it was impractical to plot them in Figure 2. They have been presented in Table II instead. The table seems to indicate that the 130-nm SRAM is more vulnerable to such large MCUs than the 90-nm and the 65-nm ones.

The shape of the MCUs has also been analyzed. Different types of 2-bit MCUs have been classified according to the shapes in Figure 3, which is a physical representation of the SRAM bitcell topology. Results are presented in Figure 4.

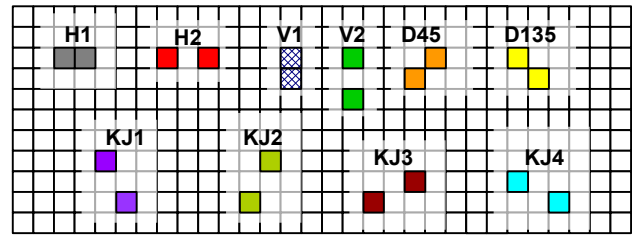


Figure 3. Classification of the observed 2-bit MCUs, according to their shapes.

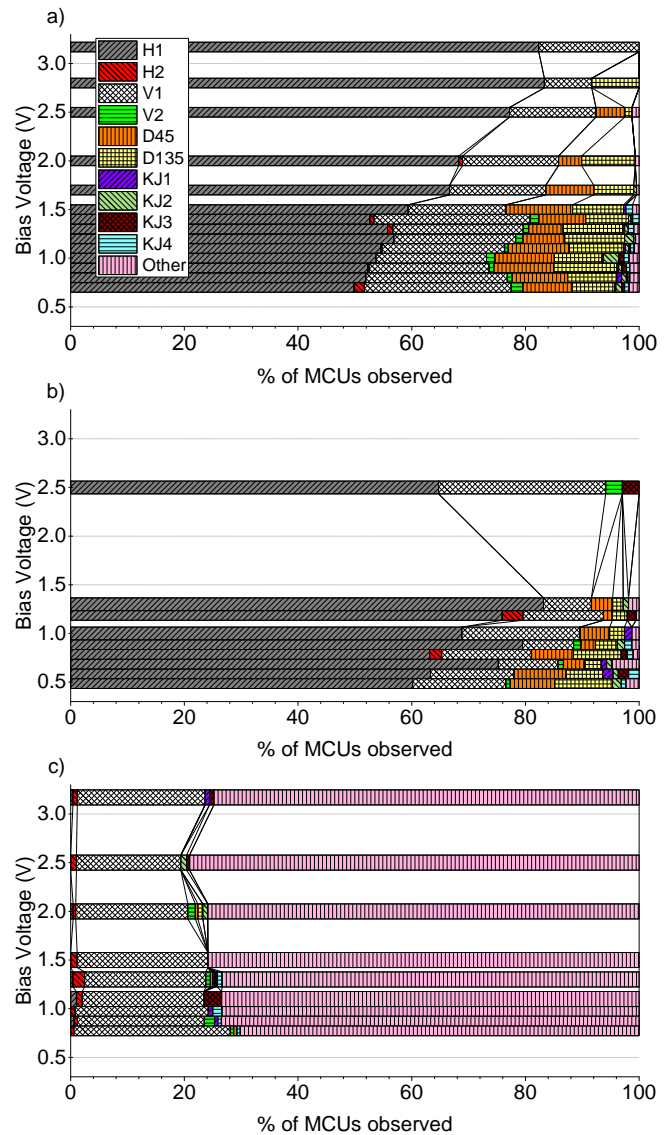


Figure 4. Shape of the 2-bit MCUs found for a) the 130-nm, b) 90-nm and c) 65-nm SRAMs at different bias voltage levels.

For each bar, percentages were calculated with respect to the number of events observed in the involved experiment. It can be observed that, for the 130-nm and 90-nm SRAMs, the most frequent 2-bit MCUs are H1, followed by V1. However, the H1 event is extremely rare in the 65-nm SRAM. The reason of this curious phenomena is that the well stripes of the CY62167GE SRAM are organized in columns, and it is

Table III
NUMBER OF READING ROUNDS WHERE μ -SELS OCCURRED / TOTAL
NUMBER OF READING ROUNDS CARRIED OUT IN THE SPECIFIED VOLTAGE
RANGE

	130 nm	90 nm	65 nm
3.15V	1/2	3/3	0/1
2.8V – 1.8V	0/3	1/2	0/2
1.7V – 1.4V	0/3	4/4	0/1
1.3V – 0.5V	0/7	0/8	0/6

very difficult to cross them because the well doping is very high. Hence, it is much more likely to observe MCUs going North to South along the well stripes. The well doping of the previous generations was weaker than that of the 65-nm one.

For the 130-nm SRAM (Figure 4a), vertical, diagonal and even knight-jump MCUs are observed more frequently at near-threshold voltage levels. This trend seems to be repeated for the 90-nm SRAM as well. In the latter case, a possible outlier may be the round performed at 2.5V, but its fluence was 2.5 times lower than that of the other rounds, in average. The reason has been pointed out above: the high susceptibility to micro-SELS in this memory at voltages above 1.4V, which made very difficult to obtain "clean" results in those cases. Besides, as a consequence of this, it was impossible to perform a round of reading free of micro-SELS at nominal voltage with this SRAM (hence the absence of that result in Figure 4b).

Finally, it is also remarkable the fact that the 65-nm SRAM behaves completely differently. Not only are horizontal MCUs very rare (indicated above), but also most of them are classified as "others". These are 2-bit events whose affected bitcells are separated by a Manhattan distance greater than 3. This may be due to the high doping existing between adjacent cells, which makes very unlikely for KJ-type events and D-type events to appear. In this case, the shape of the 2-bit MCUs does not seem to be highly determined by the SRAM bias voltage.

B. Large-Scale Events and Multiple Bit Upsets

As previously hinted in Figure 1, large-scale events, attributed to micro-SELS, were detected for the 90-nm and 130-nm SRAMs, but not for the 65-nm one.

Table III summarizes the number of reading rounds where such events were found. For the sake of clarity, they are highlighted in bold font in the table. As previously discussed (Figure 1), a micro-SEL that affected several thousands of addresses was observed in the 130-nm SRAM at nominal voltage, but this phenomena did not show up at lower bias voltages. However, the 90-nm SRAM turned out to be extremely sensitive to such large-scale events, but only at bias voltages above 1.3 V. This issue was not observed for the 65-nm one.

Single Event Functional Interrupts (SEFIs) and Multiple Bit Upsets (MBUs) were also found (Figure 5). For the 130-nm SRAM, below 1.8 V, strange clusters of 4-bit MBUs started to appear. They were attributed to SEFIs occurred in the readout system of the SRAM for three reasons: First, many common addresses were affected in all the involved rounds of reading. Second, they appeared only at bias voltages lower than 1.9 V, which is actually the threshold voltage from which the

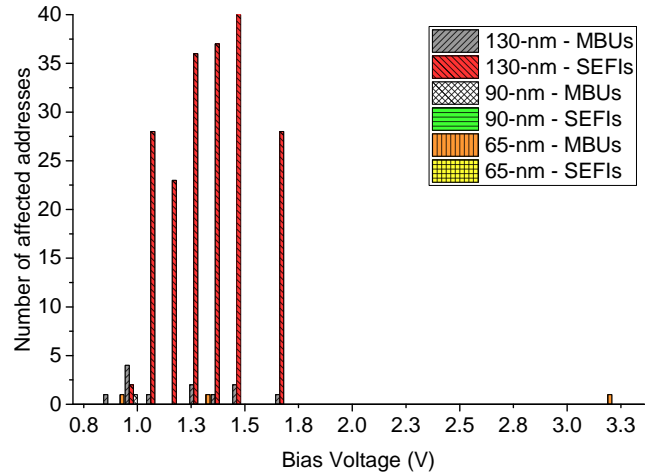


Figure 5. Number of addresses affected by MBUs and SEFIs.

readout system of the SRAM stops working (although it still retains information). And last but not least, that SRAM did not exhibit the behavior of micro-SELS, which was described in the previous section. Such SEFIs related to the readout system did not appear for the 90-nm and 65-nm ones.

Finally, a few isolated 2-bit MBUs were also observed, for the three SRAMs. However, they appeared in experiments where more than 1500 events were observed, hence they could actually be two separated SBUs occurred in the same address. Probabilistic models developed by the authors, not included in this paper for simplicity, predict a number of occurrences of these MBUs that is on the order of the number of MBUs that were observed in the experiments. For instance, in the experiment with the 65-nm SRAM at 2.5V, a 2-bit MBU was observed among 1711 bitflips. In this case, the probabilistic model predicted that 0.64 MBUs attributed to the occurrence of two SBUs in the same word should have been observed.

C. Efficiency of the ECC Mechanism of the CY62167GE30-4

The efficiency of the ECC logic implemented in the 65-nm SRAM has also been evaluated. For that purpose, another scan for different bias voltages on the same CY62167GE30-4 sample was carried out, but this time keeping the ECC active. In this case, when a read operation is performed on a position with data affected by a SBU, the "ECC" pin of the memory is automatically activated and the error is fixed by the hardware of the chip. However, it may happen that some errors escape the ECC mechanism, such as MBUs or errors occurred in the memory elements of the ECC logic. These errors are all through accumulation effects. The number of accumulated errors must be lower than 1000 for the ECC to be clean [16]. In these cases, the ECC signal is also activated, but the error is not corrected.

Table IV shows these results performed at various bias voltages. All the rounds were performed with pattern 0×55, except the last one, performed with 0×00. In all the cases, the ECC mechanism proved to be extremely effective since, at least, 99.4% of the errors were corrected. In addition, no micro-SELS were observed in this sample, in spite that it was

Table IV
ROUNDS OF IRRADIATION PERFORMED ON THE CY62167GE30-4 SRAM (65-nm), WHILE KEEPING THE ECC MECHANISM ACTIVATED

VCC (V)	Fluence ($n \cdot cm^{-2}$)	Correctable errors	Uncorrectable errors	% ECC correction
0.80	2.73×10^9	3479	20	99.43%
0.90	2.66×10^9	2799	8	99.71%
1.00	2.73×10^9	2539	9	99.65%
1.10	2.79×10^9	2373	6	99.74%
1.30	2.66×10^9	2012	1	99.95%
1.50	2.73×10^9	2015	2	99.90%
2.00	2.79×10^9	2044	3	99.85%
2.50	2.79×10^9	2038	7	99.65%
3.15	2.73×10^9	1970	5	99.74%
3.15 ^a	2.73×10^9	2062	2	99.90%

^aPerformed with pattern 0×00

the most exposed one against radiation in the whole campaign performed in May'2017 ($6.63 \cdot 10^{10} n \cdot cm^{-2}$), in comparison to the 130-nm ($3.26 \cdot 10^{10} n \cdot cm^{-2}$) and 90-nm ($2.83 \cdot 10^{10} n \cdot cm^{-2}$) ones. This is a clear evidence that this memory can work reliably in a harsh environment where radiation is a major concern.

D. SER Predictions by the MUSCA-SEP³ Tool

This subsection discusses the impact of ultra-low bias voltage for the three studied technological nodes for an avionic environment, addressing particularly MCU rates and contributions induced by neutrons, protons and muons. Indeed, the sensitivity against SEEs of nanoscale devices is expected to increase with the integration scale, and recent studies have demonstrated the occurrence of SEEs due to protons and muons [19], [20], [21]. Thus, this section presents Soft Error Rate (SER) calculations based on MUSCA SEP³ [13], which have been obtained by using the SEU models that have been validated above (Subsection IV-A) and atmospheric radiation fields composed by neutron, proton and muon spectra calculated by using ATMORAD [22]. This tool is based on simulations of extensive air showers, primary spectra model (force-field approximation [23]) and neutron spectrometer network [24].

Figure 6 presents the calculated MCU rate obtained by considering each technological node and bias voltages ranging from 0.5 to 3.3 V. The bias voltage and the integration decreases induce an increase in the MCU impact. It is also interesting to investigate the neutron, proton and muon contribution to the SER as a function of the integration node and the bias voltage. Thus, Figure 7 demonstrates that the main contribution for the three technological nodes is due to neutrons, but the technological integration and increasingly low bias voltages induce a significant contribution of protons and muons.

Previous results [20] have demonstrated that muon and α -SER impacts are negligible for avionic altitudes, and for integration levels down to 14nm considering bulk, FDSOI and FinFET processes. However, only nominal bias voltages

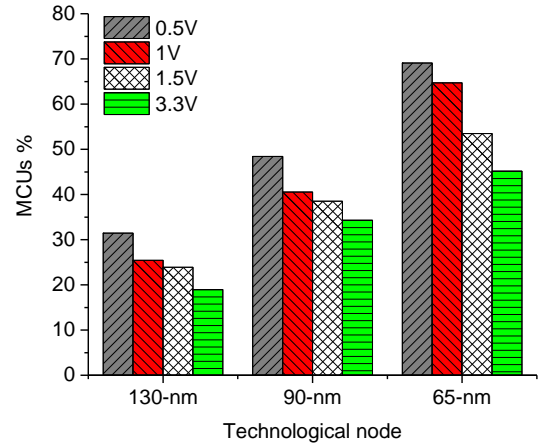


Figure 6. Estimated MCU rate versus technological node and bias voltage, considering the avionic altitude (i.e. 12 km).

Table V
MAIN TECHNOLOGICAL PARAMETERS

Node	$S_{cell} (\mu m^2)$	$Q_{crit} (fC)$	VCC (V)
65 nm	0.55	0.60	0.90
45 nm	0.40	0.40	0.85
32 nm	0.25	0.30	0.80
28 nm	0.20	0.20	0.70
22 nm	0.15	0.12	0.70
14 nm	0.10	0.08	0.50

were considered. Thus, based on the technological parameters detailed in [20], the impact of the technology scaling on the SER contributions due to these different particles was also investigated by using MUSCA-SEP³ at various bias voltages. Taking into account the integration level, interactions of primary and/or secondary particles in active silicon layers consider 3D morphology descriptions of deposited charges [21], [25]. SEU occurrence models are based on radiation ground tests for 130, 90 and 65 nm, while extended models were considered for lower integration technologies. As previously, atmospheric radiation fields were calculated by using ATMORAD. Table V describes the main technological model parameters that were used [26], [27]; i.e., the elementary cell surface (S_{cell}), the critical charge to provoke a SEU (Q_{crit}) and the nominal power supply (VCC).

Finally, Figure 8 presents neutrons, protons and muons contribution to SER versus technological node considering nominal bias voltage and avionic altitudes. Depending on the integration level, neutron and/or the proton environments induce the main contribution to the total SER, whereas that of muons is negligible. However, proton direct ionization is classically not considered as a source of SEEs for avionic applications. Complementary analyses show that the proton environmental impact is already not negligible for the 65-nm technology and indeed, it becomes the main contribution from the 28/22-nm nodes and beyond. Previous results presented by Barak et al. [28] and based on an analytical microdosimetry model, show that for low-SEU sensitivity devices, the combined contribution of secondary protons and deuterons

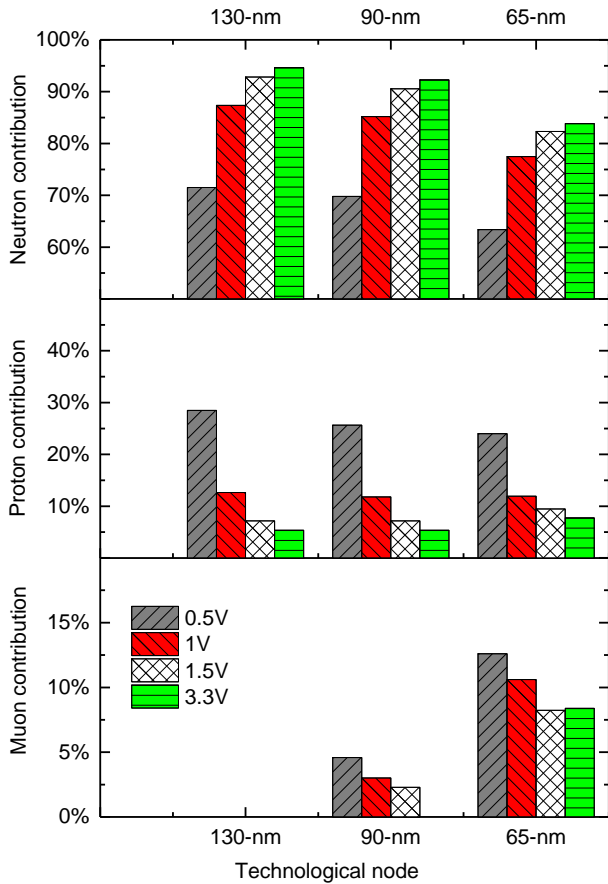


Figure 7. Estimated neutron, proton and muon contribution to SER versus technological node and bias voltage, considering the avionic altitude (i.e. 12 km).

is the dominant one. Moreover, that of muons and pions is negligible even at sea level. Results are consistent with [28].

Previous works [29] have emphasized that the technological integration for over 90-nm induces a SER saturation (or even a slight reduction) coupled with an increase of the multiple event rates. However, accounting for the direct proton ionization contribution leads to an expected strong increase in the SER at 28-nm and beyond.

By considering only the neutron contribution, the SER decreases with the downscaling despite the increase of multiple effects. This trend is reversed by proton contributions.

V. CONCLUSIONS

This paper has presented a sensitivity characterization of three successive COTS SRAMs (130-nm, 90-nm and 65-nm), manufactured by Cypress Semiconductor, against 14.2 MeV neutrons at ultra low bias voltage. A clear evidence of the sensitivity increase of these devices at very low bias voltages has been observed for single and multiple events with various multiplicities, which have been extracted with proprietary information from the manufacturer. These experimental data have been validated with predictions issued from the MUSCA-SEP³ modeling tool, and the agreement is very satisfactory.

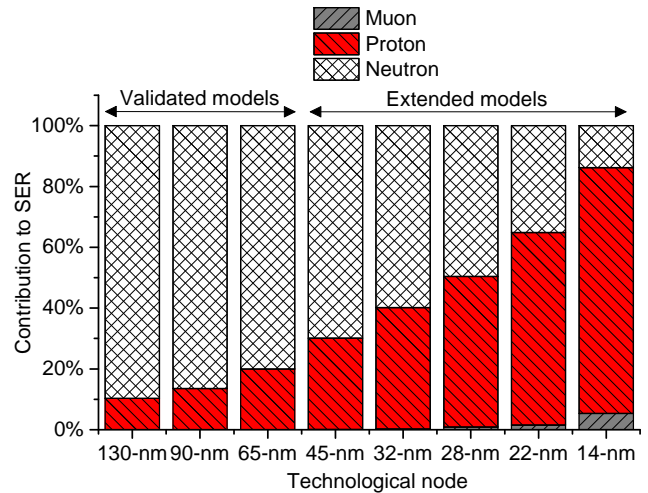


Figure 8. Neutron, proton and muon contribution to SER versus technological node considering nominal bias voltage and avionic altitudes (i.e. 12 km).

Large-scale SEFIs, micro-SEIs as well as some isolated MBUs were also reported. SER estimations, also issued from MUSCA-SEP³ and ATMORAD, have also been provided and discussed.

REFERENCES

- [1] S. Kiamehr, M. Ebrahimi, M. S. Golanbari, and M. B. Tahoori, "Temperature-aware dynamic voltage scaling to improve energy efficiency of near-threshold computing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, pp. 2017–2026, July 2017.
- [2] A. P. Chandrakasan and R. W. Brodersen, "Minimizing power consumption in digital CMOS circuits," *Proceedings of the IEEE*, vol. 83, pp. 498–523, Apr. 1995.
- [3] H. Qiu, K. Takeuchi, T. Mizutani, Y. Yamamoto, H. Makiyama, T. Yamashita, H. Oda, S. Kamohara, N. Sugii, T. Saraya, M. Kobayashi, and T. Hiramoto, "Statistical Write Stability Characterization in SRAM Cells at Low Supply Voltage," *IEEE Transactions on Electron Devices*, vol. 63, pp. 4302–4308, Nov. 2016.
- [4] T. Hiramoto, "Ultra-low-voltage Operation: Device Perspective," in *Proceedings of the 17th IEEE/ACM International Symposium on Low-power Electronics and Design, ISLPED '11*, (Piscataway, NJ, USA), pp. 59–60, IEEE Press, 2011.
- [5] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Transactions on Nuclear Science*, vol. 58, pp. 2097–2102, Aug. 2011.
- [6] H. Liu, M. Cotter, S. Datta, and V. Narayanan, "Soft-Error Performance Evaluation on Emerging Low Power Devices," *IEEE Trans. Device Mater. Rel.*, vol. 14, pp. 732–741, June 2014.
- [7] A. Hasanbegovic and S. Aunet, "Heavy Ion Characterization of Temporal-, Dual- and Triple Redundant Flip-Flops Across a Wide Supply Voltage Range in a 65 nm Bulk CMOS Process," *IEEE Transactions on Nuclear Science*, vol. 63, pp. 2962–2970, Dec. 2016.
- [8] Q. Wu, Y. Li, L. Chen, A. He, G. Guo, S. H. Baeg, H. Wang, R. Liu, L. Li, S. J. Wen, R. Wong, S. Allman, and R. Fung, "Supply Voltage Dependence of Heavy Ion Induced SEEs on 65 nm CMOS Bulk SRAMs," *IEEE Transactions on Nuclear Science*, vol. 62, pp. 1898–1904, Aug. 2015.
- [9] J. A. Clemente, F. J. Franco, F. Villa, M. Baylac, P. Ramos, V. Vargas, H. Mecha, J. A. Agapito, and R. Velazco, "Single Events in a COTS Soft-Error Free SRAM at Low Bias Voltage Induced by 15-MeV Neutrons," *IEEE Transactions on Nuclear Science*, vol. 63, pp. 2072–2079, Aug. 2016.
- [10] J. A. Clemente, G. Hubert, F. J. Franco, F. Villa, M. Baylac, H. Mecha, H. Puchner, and R. Velazco, "Sensitivity Characterization of a COTS 90-nm SRAM at Ultralow Bias Voltage," *IEEE Transactions on Nuclear Science*, vol. 64, pp. 2188–2195, Aug. 2017.

- [11] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. A. Reed, R. D. Schrimpf, J. K. Wang, N. Vedula, B. Bartz, and C. Monzel, "Impact of Technology Scaling on SRAM Soft Error Rates," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 3512–3518, Dec. 2014.
- [12] F. Villa, M. Baylac, S. Rey, O. Rossetto, W. Mansour, P. Ramos, R. Velazco, and G. Hubert, "Accelerator-Based Neutron Irradiation of Integrated Circuits at GENEPI2 (France)," in *IEEE Radiation Effects Data Workshop (REDW)*, pp. 53–57, July 2014.
- [13] G. Hubert, S. Duzellier, C. Inguibert, C. Boatella-Polo, F. Bezerra, and R. Ecoffet, "Operational SER Calculations on the SAC-C Orbit Using the Multi-Scales Single Event Phenomena Predictive Platform (MUSCA-SEP³)," *IEEE Transactions on Nuclear Science*, vol. 56, pp. 3032–3042, Dec. 2009.
- [14] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel, J. Mekki, M. Brugger, F. Wrobel, and F. Saigné, "An SRAM Based Monitor for Mixed-Field Radiation Environments," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 1663–1670, Aug. 2014.
- [15] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel, H. Puchner, C. Frost, F. Wrobel, and F. Saigné, "Multiple Cell Upset Classification in Commercial SRAMs," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 1747–1754, Aug. 2014.
- [16] J. Tausch, D. Sleeter, D. Radaelli, and H. Puchner, "Neutron Induced Micro SEL Events in COTS SRAM Devices," in *2007 IEEE Radiation Effects Data Workshop*, pp. 185–188, July 2007.
- [17] R. Velazco, J. A. Clemente, G. Hubert, W. Mansour, C. Palomar, F. J. Franco, M. Baylac, S. Rey, O. Rossetto, and F. Villa, "Evidence of the Robustness of a COTS Soft-Error Free SRAM to Neutron Radiation," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 3103–3108, Dec. 2014.
- [18] R. Pawlowski, J. Crop, M. Cho, J. Tschanz, V. De, T. Fairbanks, H. Quinn, S. Borkar, and P. Y. Chiang, "Characterization of radiation-induced SRAM and logic soft errors from 0.33V to 1.0V in 65nm CMOS," in *2014 IEEE Proceedings of the Custom Integrated Circuits Conference (CICC)*, pp. 1–4, Sept. 2014.
- [19] B. D. Sierawski, J. A. Pellig, R. A. Reed, R. D. Schrimpf, K. M. Warren, R. A. Weller, M. H. Mendenhall, J. D. Black, A. D. Tipton, M. A. Xapsos, R. C. Baumann, X. Deng, M. J. Campola, M. R. Friendlich, H. S. Kim, A. M. Phan, and C. M. Seidleck, "Impact of low-energy proton induced upsets on test methods and rate predictions," *IEEE Transactions on Nuclear Science*, vol. 56, pp. 3085–3092, Dec. 2009.
- [20] G. Hubert, L. Artola, and D. Regis, "Impact of scaling on the soft error sensitivity of bulk, FDSOI and FinFET technologies due to atmospheric radiation," *Integration, the VLSI Journal*, vol. 50, no. Supplement C, pp. 39 – 47, 2015.
- [21] G. Hubert, P. L. Cavoli, C. Federico, L. Artola, and J. Busto, "Effect of the Radial Ionization Profile of Proton on SEU Sensitivity of Nanoscale SRAMs," *IEEE Transactions on Nuclear Science*, vol. 62, pp. 2837–2845, Dec. 2015.
- [22] G. Hubert and A. Cheminet, "Radiation Effects Investigations Based on Atmospheric Radiation Model (ATMORAD) Considering GEANT4 Simulations of Extensive Air Showers and Solar Modulation Potential," *Radiation Research*, vol. 184, no. 1, pp. 83–94, 2015.
- [23] P. M. O'Neill, "Badhwar-O'Neill 2010 Galactic Cosmic Ray Flux Model - Revised," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 3148–3153, Dec. 2010.
- [24] G. Hubert, "Analyses of cosmic ray induced-neutron based on spectrometers operated simultaneously at mid-latitude and antarctica high-altitude stations during quiet solar activity," *Astroparticle Physics*, vol. 83, no. Supplement C, pp. 30 – 39, 2016.
- [25] P. L. Cavoli, G. Hubert, and J. Busto, "Study of atmospheric muon interactions in Si nanoscale devices," *Journal of Instrumentation (JINST)*, vol. 12, no. 12, p. P12021, 2017.
- [26] B. D. Sierawski, R. A. Reed, M. H. Mendenhall, R. A. Weller, R. D. Schrimpf, S. J. Wen, R. Wong, N. Tam, and R. C. Baumann, "Effects of Scaling on Muon-Induced Soft Errors," in *2011 International Reliability Physics Symposium (IRPS)*, pp. 3C.3.1–3C.3.6, April 2011.
- [27] International Technology Roadmap for Semiconductors (ITRS), "http://www.itrs2.net/," 2016.
- [28] J. Barak and N. M. Yitzhak, "SEU Rate in Avionics: From Sea Level to High Altitudes," *IEEE Transactions on Nuclear Science*, vol. 62, pp. 3369–3380, Dec. 2015.
- [29] P. Hazucha, T. Karnik, J. Maiz, S. Walstra, B. Bloechel, J. Tschanz, G. Dermer, S. Hareland, P. Armstrong, and S. Borkar, "Neutron Soft Error Rate Measurements in a 90-nm CMOS Process and Scaling Trends in SRAM from 0.25-/spl mu/m to 90-nm Generation," in *2003 IEEE International Electron Devices Meeting (IEDM)*, pp. 523–526, Dec. 2003.