Inherent Uncertainty in the Determination of Multiple Event Cross Sections in Radiation Tests

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Abstract

In radiation tests on SRAMs or FPGAs, two or more independent bitflips can be misled with a multiple event if they accidentally occur in neighbor cells. In the past, different tests such as the "birthday statistics" have been proposed to estimate the accuracy of the experimental results. In this paper, simple formulae are proposed to determine the expected number of false 2-bit and 3-bit MCUs from the number of bitflips, memory size and the method used to search multiple events. These expressions are validated using Monte Carlo simulations and experimental data. Also, a technique is proposed to refine experimental data and thus partially removing possible false events. Finally, it is demonstrated that there is a physical limit to determine the cross section of memories with arbitrary accuracy from a single experiment.

Index Terms

Birtdhay Statistics, FPGA, SEU, SRAM

I. Introduction

STATIC radiation tests on SRAMs or FPGAs are usually done by writing a known pattern in the memory, then exposing the device to some kind of radiation (protons, neutrons, heavy ions...) and finally reading the content looking for discrepancies between the initial and the final information. Thus, bitflips are located in an intermingled set of logical addresses from which Single Bit Upsets (SBUs) and Multiple Cell Upsets (MCUs) must be separated. Multiple Bit Upsets (MBUs), which consist in several bitflips along a unique word, can also be found. The popularization of bit interleaving has minimized the occurrence of this kind of event.

In the literature, there have been proposed two kinds of strategies to group bitflips into SBUs and MCUs in radiation experiments: Knowledge of the physical layout of the memory or search of statistical anomalies. In the first case, proprietary information about the layout must be provided by the manufacturer in order to create a function relating the logical address of the flipped cell with the physical position on an XY-plane. Thus, two flipped cells separated by a distance lower than a threshold value will be considered as originated in a single particle impact. This technique has been proved in many occasions and is easy to find in the literature [1]–[3].

The second option consists in combining logical addresses in pairs (e.g., XORing [4] or subtracting [5]) to detect the resulting values that occur more often than expected and, thus, pointing out to the existence of potential MCUs. Anomalously repeated values are used to combine addresses in pairs and, this way, discover hidden related bitflips [6], [7]. The main advantage of this technique is that it is not necessary to have access to any proprietary information about the memory layout. Thus, just the collection of enough experimental data allows discovering anomalously repeated values that help to organize the bitflips into SBUs and MCUs.

Yet any followed strategy presents intrinsic errors. As the number of SBUs grows, also does the probability of two independent SBUs near each other being erroneously classified as a multiple event. In 2009, Tausch applied the *"birthday statistics"* model to deduce a simple formula providing the probability of misleading pairs of SBUs with 2-bit MCUs and backed up his deductions with results on apparent MBUs in an irradiated FPGA [8]. This model has been widely used since its publication in order to test the accuracy of experimental multiple-event cross sections [5], [9]–[13]. Recently, the authors related the birthday statistics with the expected number of false pairs of events according to the classical *"Urn-and-balls"* problem [14]. Thus, the expected number of false MBUs and of false 2-bit MCUs can be determined, provided that the memory size, the word width and the number of bitflips are known. This technique is also valid for radiation test campaigns on SRAM-based FPGAs.

This paper proposes mathematical expressions to determine the expected number of false 2-bit and 3-bit MCUs in datasets from radiation experiments whichever the method to classify errors is. Mathematical predictions are supported by Monte Carlo simulations and by experimental data. Finally, it is discussed how to make the experimental results more accurate even though there is a physical limit that avoids knowing the cross section with arbitrary accuracy from a single experiment. This manuscript explores in depth the results shown in a paper that we presented in RADECS 2019 [15].

TABLE I
LIST OF PARAMETERS OF THE MEMORY

Parameter	Meaning	Note
L_N	Memory size in bits	
N	Number of bits to codify L_N	$2^{N-1} < L_N \leq 2^N$
W	Word width in bits	
N_W	Number of bits to codify W	$W = 2^{N_W}$
L_A	Number of word addresses	$L_A = L_N/W$
N_A	Number of bits to codify L_A	$2^{N_A-1} < L_A \leq 2^{N_A}$
N_{SB}	Number of SBUs	
N_{Mk}	Number of k-size mult. events	
N_{BF}	Number of total bitflips	

II. ESTIMATING THE NUMBER OF FALSE EVENTS

First of all, let us suppose that an SRAM or SRAM-based FPGA with the characteristics in Table I is tested under radiation and that, once completed the test, there are N_{BF} bitflips in the set of logical addresses $A = \{a_1, a_2, \ldots, a_{NBF}\}$.

It is easy to deduce that the number of possible pairs (a_i, a_j), with $a_i < a_j$ is:

$$N_P = \begin{pmatrix} N_{BF} \\ 2 \end{pmatrix} = \frac{1}{2} \cdot N_{BF} \cdot (N_{BF} - 1) \tag{1}$$

In the literature, there are several methods [8], [14] to determine if the addresses (a_i, a_j) are independent of each other or belong to the same multiple event. Some of them are:

1) *MBUs*: Bitflips are related if they belong to the same word. This method is less interesting in modern SRAMs due to the use of bit interleaving.
2) *Manhattan Distance (MD)*: If somehow the logical address can be associated with the physical one, bitflips are placed on an XY-plane ($a_i \rightarrow (x_i, y_i)$, $a_j \rightarrow (x_j, y_j)$) and are related if the Manhattan Distance between them is equal or lower than D:
$$d_{MD}(a_i, a_j) = |x_i - x_j| + |y_i - y_j| \leq D \tag{2}$$
3) *Infinite Norm Distance (IND)*: Similar to the latter, but with:
$$d_{IND}(a_i, a_j) = \max\left(|x_i - x_j|, |y_i - y_j|\right) \leq D \tag{3}$$
4) *Threshold Distance (TD)*: (a_i, a_j) are related if $|a_i - a_j| < T$.

Methods 2 & 3 will be called *"geometric methods"* in this paper. Method 4 is not truly geometric since it works with logical addresses and not with physical ones. It has been used, for example, with FPGA bitstreams. Finally, there also exist the so-called *"statistical methods"*, in which anomalies in the characteristics of the pairs of hit addresses need to be discovered. Two examples [6], [7] are:

5) *Statistical Anomalies for XOR*: Pairs of addresses can be bitwise XORed in order to create a new set, DV. If there are only SBUs, it is possible to determine the number of expected repetitions of elements in DV. If there are anomalously repeated, or critical, elements, $X = \{x_1, x_2, \ldots, x_m\}$, pairs of related addresses are found if $a_i \oplus a_j \in X$.
6) *Statistical Anomalies for POS (Positive Subtraction)*: Identical to the previous one but using *POS*, $|a_i - a_j| = r_k \in R$, R being the set of critical values.

Geometrical methods (2 & 3) require a deep knowledge of the internal layout of the device. On the contrary, methods 1 & 4-6 are interesting for experiments in which only the logical address is known, 5 being appropriate for discrete SRAMs and 4 & 6 for FPGAs.

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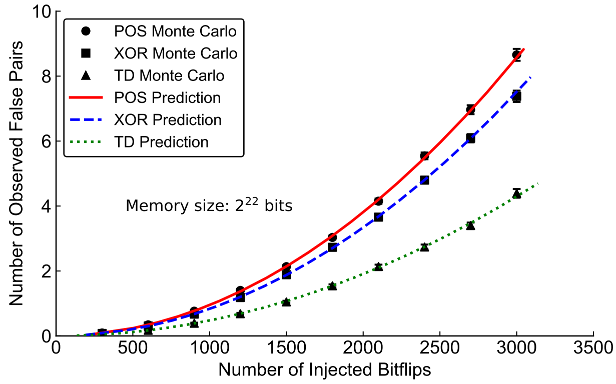

Fig. 1. Monte Carlo simulation of a memory where SBUs were randomly injected and anomalous values for the DV sets (both for PS and XOR) were looked for. The number of trials ranged from 5000 with 300 bitflips to 1000 with 3000 bitflips. Symbols represent the average number of false detected MCUs and error bars indicate the 95%-confidence range. Lines are related to (7), (9), and (10), respectively.

A. False 2-bit multiple events

Previous studies [8], [14] have proposed equations to estimate the expected number of false 2-bit MCUs, when geometric methods are used to group bitflips in multiple events:

$$\text{MBUs:} \qquad N_{FM2} \simeq L_N^{-1} \cdot N_P \cdot (W-1) \tag{4}$$

$$\text{MD:} \quad N_{FM2} \simeq L_N^{-1} \cdot N_P \cdot 2 \cdot D \cdot (D+1) \tag{5}$$

$$\text{IND:} \quad N_{FM2} \simeq L_N^{-1} \cdot N_P \cdot 4 \cdot D \cdot (D+1) \tag{6}$$

$$\text{TD:} \qquad N_{FM2} \simeq L_N^{-1} \cdot N_P \cdot 2 \cdot (T-1) \tag{7}$$

In these expressions, N_P must be calculated using N_{SB} instead of N_{BF} since only SBUs are of interest. If N_{BF} were used, previous expressions would only provide a very pessimistic prediction that, at any rate, can be interesting enough to the researcher if the values allow ruling out the occurrence of false events. Let us note that (7) is a slightly corrected version of the one derived from the birthday-statistics test [8], [14] to exclude the central cell ($T = 0$).

Recently, in [16] the authors needed to determine the ratio between false and actual 2-bit MCU. They identified pairs with the IND with $D = 1$ and proposed an expression quite similar to (6) although an erroneous additional factor of 2 was added due to not having correctly counted the number of SBU pairs. At any rate, the conclusions of this manuscript are by no means invalidated.

Methodologies for estimating such number of false 2-bit MCUs have not yet been explored in the literature. Both the XOR and POS operations yield values between 1 and $L_X - 1$, L_X being either L_N or L_A depending on using cell or word addresses to determine the anomalous values. Applying the probability theory, if P_k is the probability of getting $k \in [1, 2, \ldots, L_X - 1]$, the number of false 2-bit events is:

$$N_{FM2} = N_P \cdot \sum_{k \in R} P_k \tag{8}$$

In previous works [6], [7], it was demonstrated that for the XOR operation $P_k = (L_X - 1)^{-1} \simeq L_X^{-1}$ and for POS $P_k \simeq 2 \cdot L_X^{-1} \cdot (1 - k/L_X)$. Using this in Eq. 8:

$$\text{XOR:} \qquad N_{FM2} = L_X^{-1} \cdot N_P \cdot m_X \tag{9}$$

$$\text{POS:}\ N_{FM2} = L_X^{-1} \cdot N_P \cdot 2 \cdot m_R \cdot \left(1 - \sum_{k=1}^{m_R} r_k \cdot L_X^{-1}\right) \tag{10}$$

m_X and m_R being respectively the number of elements in DV for the XOR and POS operators, as previously explained.

Unlike Eqs. 4-6, already tested in [14], (7), (9) & (10) need to be verified. Thus, a Monte Carlo analysis was performed injecting random SBUs in a simulated 4-Mb memory. Next, flipped addresses were combined in pairs to apply the TD, XOR and PS methods, and then it was counted: a) the number of pairs separated no farther than $T = 3$; b) those that, after being XORed, yielded 2^k, $k \in [0, 1, \ldots, 6]$ ($m_X = 7$); c) those that, after being subtracted, yielded one element in $R = \{1, 2047, 2048, 2049\}$ ($m_R = 4$, this value being selected in advance). Fig. 1 compares predictions and simulations, which are in very good agreement[1].

[1]All the mathematical calculations shown in this paper, either simulations or data analysis, were done using Julia 1.1.1 [17].

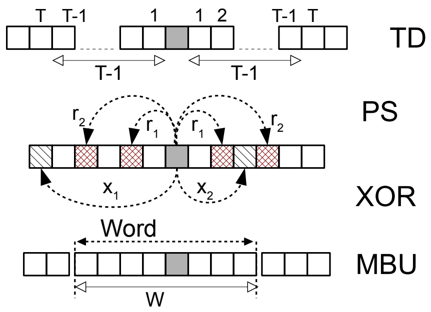

Fig. 2. Some examples of the physical origin of S_1. In the upper side, it is clear that there are $2 \cdot (T-1)$ cells in a bitstream at a distance lower than T from the central cell (grey). Below, one can see that four possible cells are associated with the central one by the positive subtraction with two values, r_1 and r_2. In general, if there are m_R anomalous values, the number of cells would be $2 \cdot m_R$ if $r_i \ll L_X$. Next, the XOR operation only links one cell per value x_i with the central cell, so $S_1 = m_X$. Finally, in the MBU search, if a cell has been hit, there are only $W-1$ additional cells in which another bitflip could lead to believe that a 2-bit MBU occurred.

TABLE II
CELL INFLUENCE AREA FOR DIFFERENT METHODS

Method	S_1	Method	S_1
MBU	$W-1$	TD	$\simeq 2 \cdot (D-1)$
MD	$\simeq 2 \cdot D\,(D+1)$	XOR	m_X
IND	$\simeq 4 \cdot D\,(D+1)$	POS	$\simeq 2 \cdot m_R$

An interesting fact is that all the equations to calculate N_{FM2} can be expressed as:

$$N_{FM2} = L_X^{-1} \cdot N_P \cdot S_1 \tag{11}$$

In [14], the factor $S_1 = 2 \cdot D \cdot (D+1)$ for the MD method was identified with the number of cells around the flipped cell at a Manhattan distance equal to or lower than D. The same occurs for IND, in which $S_1 = 4 \cdot D \cdot (D+1)$. As Fig. 2 shows, this concept can be extended to the other methods. Indeed, S_1 is just the number of cells to which the flipped cell can be related according to the method used to match pairs.

In analogy with the MD & IND methods, we will call S_1 *"Cell Influence Area"*. This definition clarifies the meaning of the factor S_1/L_X in all the expressions since it represents the fraction of the memory around the flipped cell. Other factors such as the sum in (10) are attributed to border effects. Table II summarizes the values of S_1 for the different methods. It is worth to indicate that this concept was already explored by Gasiot *et al.* in 2006 [18], who proposed a similar expression to (11) applied to the IND. However, the expression in that paper is apparently flawed since it shows an incorrect linear dependence on N_{BF}, instead of on $N_{BF} \cdot (N_{BF}-1)/2$.

B. False 3-bit Multiple Events

The idea of the cell influence area can be used to estimate the number of false 3-bit multiple events that can occur due to the random accumulation of SBUs. As in the previous section, where (1) provides the number of possible pairs, the number of triplets of flipped addresses, (a_i, a_j, a_k), with $a_i < a_j < a_k$ must be determined. This value, N_T, is just the number of possible combinations of N_{SB} elements taken in threes:

$$N_T = \binom{N_{SB}}{3} = \frac{1}{6} \cdot N_{SB} \cdot (N_{SB}-1) \cdot (N_{SB}-2) \tag{12}$$

To define a false 3-bit MCU, at least one of the addresses must be related to the other two. Let us suppose that this element is a_i. The probability of occurrence of a false 3-bit MCU is proportional to the probability of a_j falling in the influence area of a_i (S_1/L_X) and of a_k falling in any of the cells of S_1 excluding a_j ($(S_1-1)/L_X$). Thus:

$$N'_{FM3} = M \cdot L_X^{-2} \cdot S_1 \cdot (S_1-1) \cdot N_T \tag{13}$$

The occurrence of false 3-bit MCUs should lead to add a negligible correction to (8) and related, which will be deeply studied in (15) & Section IV-B. Besides, an additional parameter, M, has been added to (13) since, theoretically, the role of a_i as central SBU can be also played by a_j and by a_k. Therefore, ideally, $M = 3$. However, Monte Carlo simulations reveal that the actual value is not so easy to estimate. Fig. 3 shows the results of simulating an only-SBU system in which MCUs are detected following: a) the method of the MBUs; b) a geometric method such as the Manhattan distance; c) the statistical POS

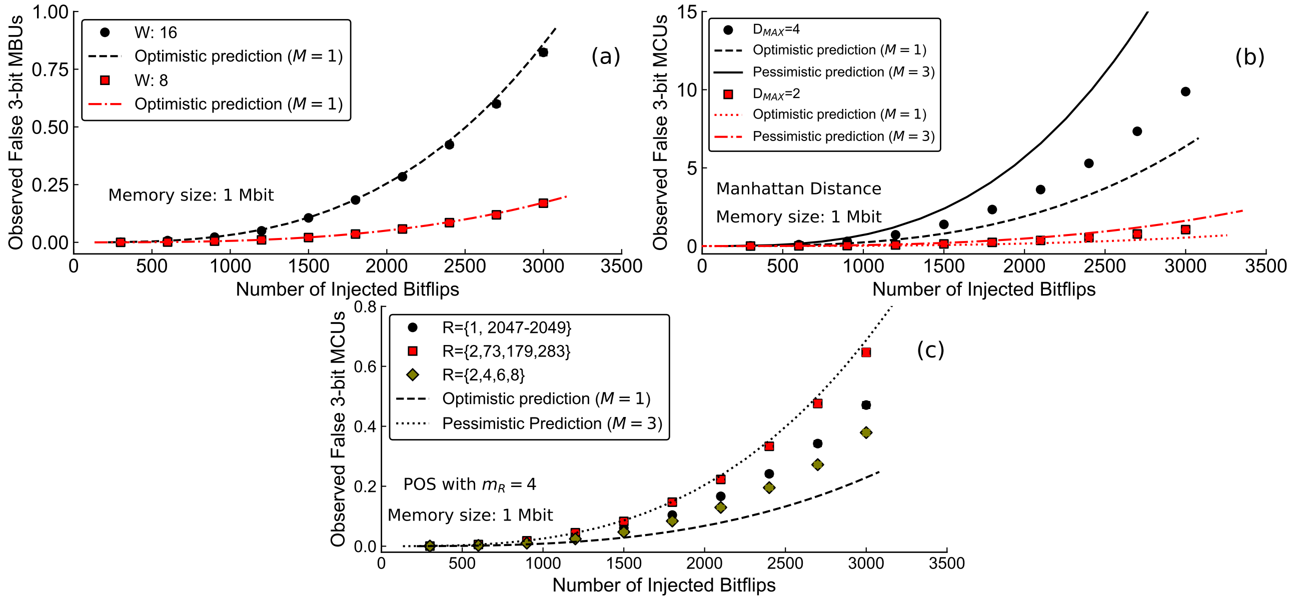

Fig. 3. Predictions of false 3-bit events from Monte Carlo simulations in a memory with 20000 trials: (a) MBUs with different widths, W; (b) Manhattan distance lower or equal than D_{MAX} ; (c) POS method with different sets of four elements. In (b), the cells were in a 1024×1024 grid.

TABLE III
2-BIT MCU INFLUENCE AREA FOR DIFFERENT METHODS

Method	S_{2S}	S_{2L}
MBU	$W-2$	$W-2$
MD	$2D^2+4D$	$2D^2+5D-1+$ $+2\cdot(D-1)\cdot div(D,2)+$ $+2\cdot div(D+1,2)\cdot(div(D+1,2)-1)$
IND	$4D^2+6D$	$7D^2+6D-1$
THD	$2T-2$	$3T-4$
XOR	$\geq m_X-1$	$\leq 2m_X-2$
POS	$\geq 2m_R-1$	$\leq 4m_R-2$

method. In practice, M ranges from 1, observed in MBUs, to 3, in the POS method whose anomalously repeated elements were four mutually prime numbers (red squares in Fig. 3c). Hereafter, the case of $M=1$ will be called *"optimistic"* and *"pessimistic"* for $M=3$. The reason of this unexpected behavior is that the influence areas of the three cells can overlap, reducing the possible combinations.

Let us investigate another mechanism that may lead to the detection of false large size events. The only-SBU model becomes more realistic assuming that not only do SBUs occur but also 2-bit MCUs. Hereafter, we will call this model as *"Single & Double Events Model" (SDEM)*. In it, one can consider that the memory has undergone N_{SB} SBUs and N_{M2} 2-bit MCUs (therefore, the total number of bitflips is $N_{BF}=N_{SB}+2\cdot N_{M2}$). A false 3-bit event will also be detected if an SBU falls near a 2-bit MCU. Like in the case of SBUs, an *"MCU influence area"*, S_2, can be defined to play an analogous role to S_1. However, there is a very important difference: this area depends on the 2-bit MCU shape, as shown in Figs. 4-6. Or, more accurately, it depends on how the individual cell influence areas of the flipped cells overlap. Therefore, assuming that S_{2S} and S_{2L} are respectively the smallest and largest influence areas that 2-bit MCUs can create, the number of false 3-bit MCUs is enclosed by:

$$N_{SB}\cdot N_{M2}\cdot S_{2S}\cdot L_X^{-1}\leq N^*_{FM3}\leq N_{SB}\cdot N_{M2}\cdot S_{2L}\cdot L_X^{-1} \qquad (14)$$

$N_{SB}\cdot N_{M2}$ being the total number of combinations of SBUs and 2-bit MCUs, and S_{2X}/L_X, the probability of interaction. It is easy to deduce that $S_1-1\leq S_{2X}\leq 2S_1-2$ whichever the method is. Table III shows more accurate values for the edges. As previously done, the values limiting N_{FM3} will be called "optimistic" (left) and "pessimistic" (right). For a specific experiment, the exact value of N^*_{FM3} depends on the ratio among the probability of occurrence of different shapes of 2-bit MCUs and, thus, a weighted average is required.

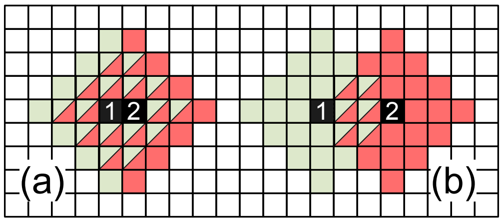

Fig. 4. Dependence of the influence area of a 2-bit MCU on the shape. Flipped bits are related if they are no farther from each other than a Manhattan distance, D. In this example, $D = 3$. In (a), flipped bits, 1 & 2 are adjacent, covering a total surface of 30 cells ($S_{2S} = 2 \cdot D^2 + 4 \cdot D$). In (b), they are separated by a distance D covering between both 40 ($S_{2L} = 2 \cdot D^2 + 5 \cdot D - 1 + 2 \cdot (D-1) \cdot k_1 + 2 \cdot k_2 \cdot (k_2 - 1)$, with $k_1 = div(D, 2)$, $k_2 = div(D+1, 2)$). In green, cells covered only by 1, in red those covered only by 2 and mixed colored by both.

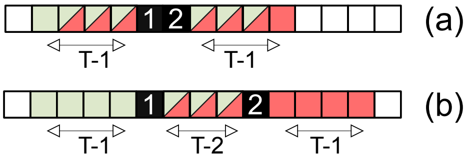

Fig. 5. Dependence of the influence area of a 2-bit MCU on the shape for threshold distance, T, in a bitstream. In this example, $T = 5$. In (a), flipped bits, 1 & 2 are adjacent, covering a total surface of $2T - 2$ cells. In (b), they are separated a distance T covering between both $3T - 4$ cells. In green, cells covered only by 1, in red those covered only by 2 and mixed colored by both. This picture is also valid for the POS method since the TD one is equivalent to POS with $R = \{1, 2, \ldots, T - 1\}$.

The total number of false 3-bit MCUs is the addition of both contributions, $N_{FM3} = N'_{FM3} + N^*_{FM3}$, also with optimistic and pessimistic limits. Fig. 7 shows the results got for an SRAM where SBUs and 2-bit MCUs were injected. For this test, N_{BF} bitflips were simulated, such that $N_{SB} = 0.8 \cdot N_{BF}$ were SBUs and $N_{M2} = 0.1 \cdot N_{BF}$ 2-bit MCUs. Figs. 7a-b correspond to geometric methods, in which 80% of the 2-bit MCUs affected adjacent cells in X, Y or diagonal axis, and 20% were cells at distance 2 in horizontal or vertical axes. In statistical methods, sets of four critical elements were used and 80% of the pairs of cell addresses were related by the first two and 20% by the other ones.

In geometric methods, as most of the events involved nearly adjacent cells with influence areas near S_{2S}, the number of false 3-bit MCUs is close to the optimistic value predicted by (14), especially at low values of injected bitflips and D_{MAX}. However, there is a significant deviation from predictions for the largest values of D_{MAX} and N_{BF}, which are explained in the following paragraphs. In statistical methods, simulations fit predictions with accuracy. In this case, the more elements of X or R that can be expressed as simple combinations of other two elements, the closer the predictions to the optimistic case. For example, the values for X_2 in Fig. 7c shift towards the optimistic case since $0 \times 101 = 0 \times 100 \oplus 0 \times 001$. On the contrary, it is impossible to XOR pairs of elements of X_1 to obtain any of the other two values of the set. This makes the simulated values for X_1 follow the pessimistic prediction.

Figs. 7c-d also show that the number of false 3-bit MCUs move away from the predicted values as N_{BF} increases. This is clearly observable in the dots corresponding to X_1 and R_1, which accurately fit the predictions with $M = 3$ for low values of N_{BF} but not for highest ones. This can be explained by the fact that, as the number of 2-bit MCUs grows, the chance of the interaction of two 2-bit MCUs, or two SBUs with a 2-bit MCU, or 4 SBUs, is not negligible. Thus, for instance, Monte Carlo simulations show that, for the IND with $D_{MAX} = 4$, the number of false 4-bit MCUs is 12.71 ± 0.05. Even more, false 7-bit MCUs were observed quite often in this particular case and, in some trials even false 11-bit MCUs appeared. In conclusion, the lower values of observed false 3-bit is related to the appearance of false multiple events of larger size.

Unfortunately, it is difficult to find expressions to estimate the expected number of larger false multiple events. The reason is that the number of possible combinations leading to a k-bit MCU increases with k, and even small MCUs can interact. Thus, the shape of both events should be taken into account making the theoretical study extremely difficult.

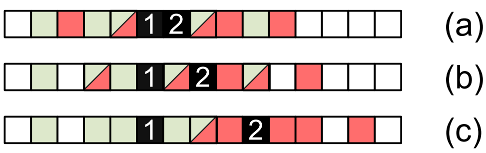

Fig. 6. Dependence of the influence area of a 2-bit MCU on the shape for POS in a bitstream. In the picture, $R = \{1, 2, 4\}$. In (a), the addresses of flipped bits, 1 & 2, differ in 1, thus covering 8 cells. In (b), the difference is 2 and the influence area is reduced to 7. However, in (c), the difference between the cells is 4 and 9 cells are at reach. In green, cells covered only by 1, in red those covered only by 2 and mixed colored by both.

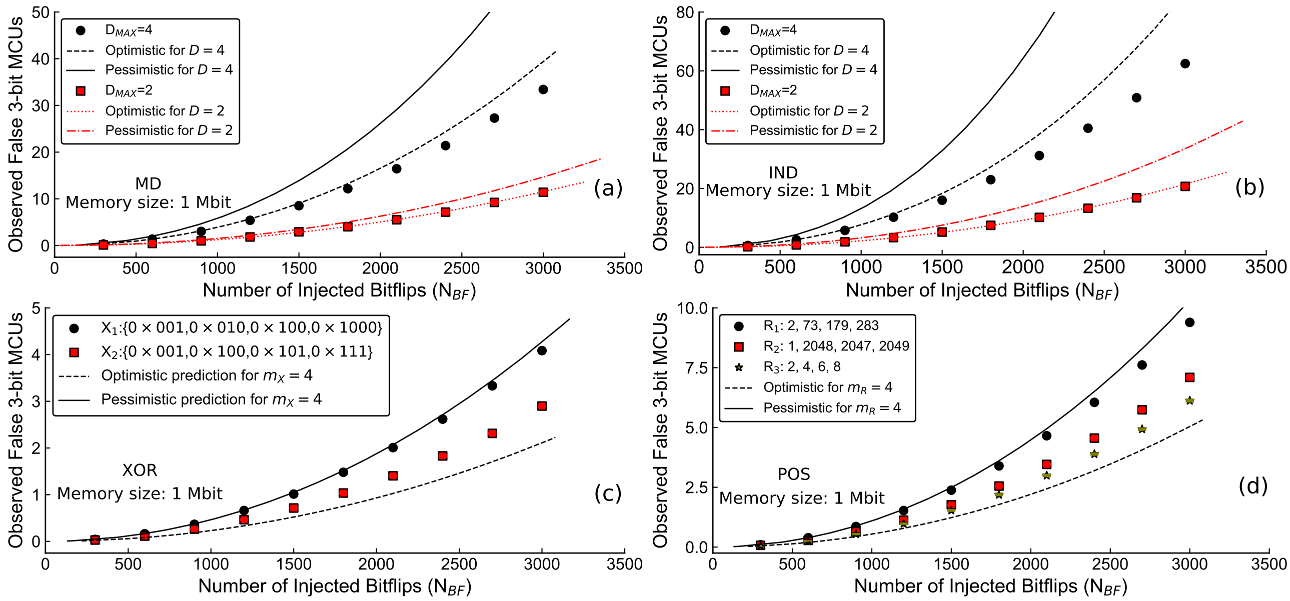

Fig. 7. Predictions of false 3-bit events from Monte Carlo simulations in a memory with 20000 trials injecting SBUs and 2-bit MCUs: (a) Manhattan distance lower or equal than D_{MAX}; (b) Idem for IND (b); (c) XOR method with different sets of four elements; (d) Idem for POS.

III. Experimental validation

Although Monte Carlo simulations have accounted for the theoretical results for false multiple events, it is necessary to take a step forward and to validate the predictions for actual experiments. Unfortunately, there is an inherent pitfall: due to the possible accumulation of false multiple events, it is extremely difficult to know from experiments the exact number of multiple events and their shapes. To avoid this limitation, an indirect approach was adopted in this paper.

Let us note O_{SB}, O_{M2}, O_{M3}, $\ldots$, the number of *observed* events after the experiment. These values can be expressed as functions of the actual ones as:

$$\begin{cases} O_{M3} &= N_{M3} + N^{*}_{FM3} + N'_{FM3} \\ O_{M2} &= N_{M2} + N_{FM2} - N^{*}_{FM3} \\ O_{SB} &= N_{SB} - 2 \cdot N_{FM2} - 3 \cdot N'_{FM3} - N^{*}_{FM3} \end{cases} \tag{15}$$

The exact values of N_X on the right side of the equations are unknown but the expected ones can be used instead to get, at least, a better approach.

In 2017, the authors reported results issued from tests under 14-MeV neutrons for a 1-M×8-bit 90-nm CMOS SRAM at different bias voltage values [3]. For these tests, the MCU detection technique was the Manhattan distance with $D_{MAX} = 2$. At a bias voltage of 1.2 V and after receiving $2.14{\cdot}10^9$ n/cm^2, 782 bitflips were observed in the SRAM that were distributed as 623 SBUs, 69 2-bit MCUs and 7 3-bit MCUs. As larger events were not observed, this dataset is appropriate to test Eq. 15. Now, we will reinterpret the experimental results changing the values of D_{MAX}. This is shown in Fig. 8, in which the Manhattan distance is increased up to 20, which is an unrealistic value but useful to verify the predictions. As expected, the number of observed SBUs decreases with the Manhattan distance whilst the number of observed multiple events grows. In each subfigure, there are two additional lines showing the least and most pessimistic predictions issued from (15) with (8), and (13) and (14), in which $M = 1$ and S_{2S} were used for the optimistic prediction and $M = 3$ and S_{2L} for the pessimistic one. Despite the approximations done, experimental results seem to be in acceptable agreement with the predictions. Slight deviations of the experimental number of false 3-bit MCUs from predictions is explained by the occurrence of up to 3 false 4-bit MCUs.

This dataset can be used to test the statistical methods, namely the XOR technique. Table IV shows 11 critical values relating pairs of *word* addresses by means of the XOR operation for this specific model of SRAM [6]. These values allow getting a good approximation to the actual distribution of events (628 SBUs, 71 2-bit MCUs, 4 3-bit MCUs) although, in [3], it was possible to improve this prediction combining the XOR and the POS operations.

Now, we will proceed as follows: First of all, elements of Table IV will be added one by one to classify the bitflips. Once the 11 values are used, the set X_1 is artificially enlarged attaching random values with no physical relevance. Fig. 9 shows that the number of observed events of each multiplicity quickly changes as the genuine first 11 elements are used until reaching the final value (628, 71, 4). From the 12th element on, the calculated numbers of SBUs and 2- and 3-bit MCUs seem to reach stable values that, however, steadily change due to the erroneous detection of falsely related bitflips, following the predictions of the SDEM.

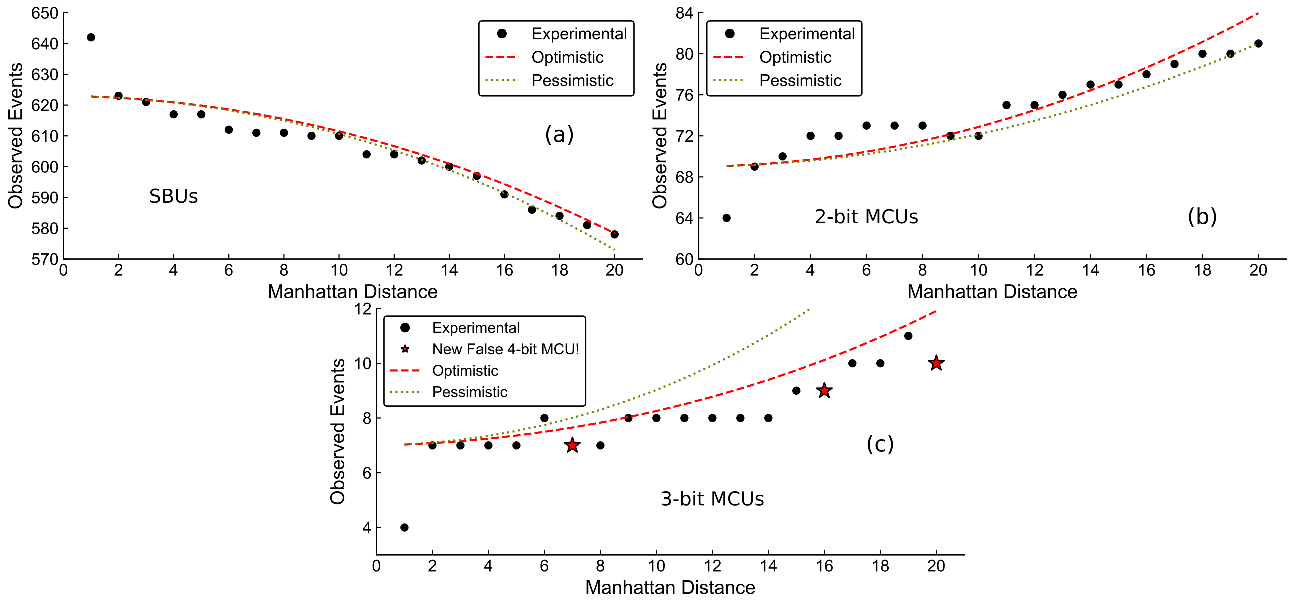

Fig. 8. Classification of 782 bitflips that appeared on radiation tests on an 8-Mbit SRAM in SBUs and multiple events as the Manhattan distance increases. Lines show the extreme predictions for expected number of observed events of each multiplicity according to the SDEM.

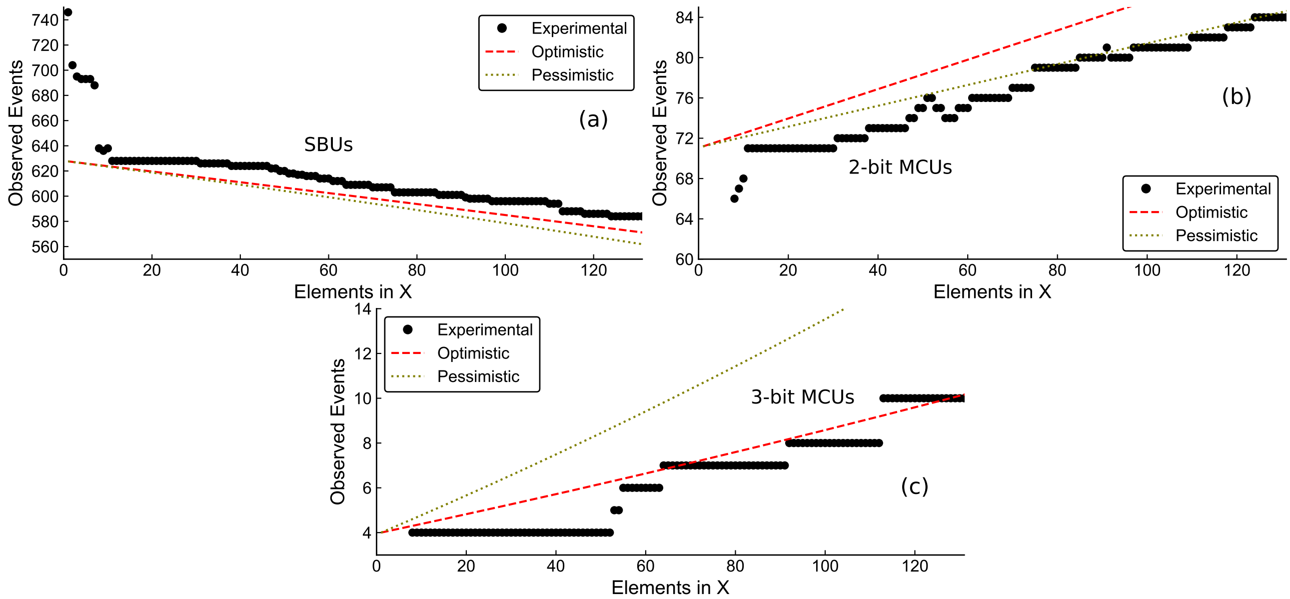

Fig. 9. Similar analysis to that of Fig. 8, but for the statistical XOR method. The first 11 elements of the X set are listed in Table IV. The rest of elements (12-132) were random numbers from 0×00000 to $0 \times FFFFF$ added one by one to the initial set of critical elements to artificially increase m_X. Lines show the extreme predictions for expected number of observed events of each family according to the SDEM.

TABLE IV
CRITICAL XOR DV VALUES FOR TESTED SRAM IN DECREASING IMPORTANCE

	Element		Element		Element
1:	$0 \times 0C000$	5:	$0 \times 0C002$	9:	0×00004
2:	$0 \times 0E000$	6:	$0 \times 0C006$	10:	0×00100
3:	0×00002	7:	0×04000	11:	0×08002
4:	0×00006	8:	0×08000		

TABLE V
PARAMETERS IN (20)

Parameter	Value	Parameter	Value
α_1	$\frac{1}{2} \cdot S_1 \cdot L_X^{-1}$	k_1	$1 + 2\alpha_1 - 6\alpha_2$
α_2	$\frac{M}{6} \cdot (S_1 - 1) \cdot S_1 \cdot L_X^{-2}$	k_2	$2\alpha_1 - 9\alpha_2$
α_3	$S_{2X} \cdot L_X^{-1}$		

IV. DISCUSSION

In previous sections, it has been proposed a method to determine the number of false multiple events in radiation tests. This allows proposing techniques to refine the raw experimental results.

A. Extension of the Birthday Statistics equations

The birthday statistics technique, proposed by Tausch in 2009 [8], has been used by researchers to test the validity of experiments since it provides the probability of erroneously identifying two SBUs as a 2-bit MCU. This technique is useful in special cases such as bitstreams in FPGAs, SRAMs, etc. In general, if it can be predicted that, in an experiment, there will be, on average, N_{FM2} false 2-bit events, the probability of observing false multiple events is [14], [18]:

$$P = 1 - \exp\left(-N_{FM2}\right) \tag{16}$$

Eq. 4 and a slightly different version of (7) can be used in (16) to get the original equations proposed by Tausch. Eqs. 5 & 6 were used as well to propose equivalent equations for geometric methods [14]. In this paper, two new equations to estimate the probability of registering false events are proposed for statistical methods:

$$\text{XOR:} \qquad P = 1 - \exp\left(-L_X^{-1} \cdot N_P \cdot m_X\right) \tag{17}$$

$$\text{POS:} \qquad P \cong 1 - \exp\left(-2 \cdot L_X^{-1} \cdot N_P \cdot m_R\right) \tag{18}$$

In last expression, the sum present in (10) has been removed since usually $r_k \ll L_X$. In general, the equation of the probability of doing erroneous detections of MCUs for whichever method is:

$$P = 1 - \exp\left(-L_X^{-1} \cdot N_P \cdot S_1\right). \tag{19}$$

B. Corrections on the observed number of events

Eq. 15 can be transformed into a nonlinear system of equations in which the number of observed X-size events, O_X, can be expressed as functions of the actual ones, N_X and on technical parameters such as L_N, M, S_1, and S_{2X}.

$$\begin{aligned} k_1 N_{SB} - 3\alpha_2 N_{SB}^3 - k_2 N_{SB}^2 - \alpha_3 N_{SB} N_{M2} &= O_{SB} \\ N_{M2} + \alpha_1 N_{SB}^2 - \alpha_1 N_{SB} - \alpha_3 N_{SB} N_{M2} &= O_{M2} \\ N_{M3} + \alpha_2 N_{SB}^3 - 3\alpha_2 N_{SB}^2 + 2\alpha_2 N_{SB} + \alpha_3 N_{SB} N_{M2} &= O_{M3} \end{aligned} \tag{20}$$

Table V shows the meaning of the different parameters. The values of M and S_{2X} range from 1 to 3 and from S_{2S} to S_{2L} depending on the researcher's choice. This system can be solved with numerical methods such as the Newton-Raphson's for several variables allowing getting refined values of the number of different kinds of events, closer to the actual values. Let us return to the example of Fig. 8 ($N_{SB} = 625$, $N_{M2} = 69$, and $N_{M3} = 7$) and choose the values for $D_{MAX} = 20$. In this situation, there were 578 apparent SBUs, 81 2-bit MCUs, 10 3-bit MCUs, and 3 4-bit MCUs. Using these values as inputs for Eq. 20 allows getting $N_{SB} = 622.2$, $N_{M2} = 66.0$, and $N_{M3} = 5.3$ with the optimistic values of M and S_{2X}, much closer to reality than the untreated ones.

Unfortunately, false 4-bit MCUs could not be corrected with the model proposed in this manuscript. It is necessary to develop, if possible, an even more refined model. Besides, the correction with the most pessimistic parameter values yields values far from actual ones ($N_{SB} = 628.8$, $N_{M2} = 68.8$, and $N_{M3} = 1.2$). The reason is that, in practice, most of the 2-bit MCUs affect adjacent cells so the MCU influence areas are closer to Fig. 4a than to other options.

C. Uncertainty at determining the actual number of events

Let an L_N-size memory be exposed to energetic particles, reaching a fluence of ϕ. Let us accept that only two kinds of events may occur: SBUs, with a cross section of σ_{SB}, and 2-bit MCUs, with σ_{M2}. The expected number of events is:

$$\overline{N}_{SB} = \sigma_{SB} \cdot L_N \cdot \phi \qquad \overline{N}_{M2} = \sigma_{M2} \cdot L_N \cdot \phi \tag{21}$$

The total expected number of bitflips is calculated as:

$$\overline{N}_{BF} = \overline{N}_{SB} + 2 \cdot \overline{N}_{M2} = (\sigma_{SB} + 2 \cdot \sigma_{M2}) \cdot L_N \cdot \phi \tag{22}$$

Hence, replacing (22) in (21):

$$\overline{N}_{SB} = \frac{\sigma_{SB}}{\sigma_{SB} + 2 \cdot \sigma_{M2}} \cdot \overline{N}_{BF} = \alpha_1 \cdot \overline{N}_{BF} \tag{23}$$

$$\overline{N}_{M2} = \frac{\sigma_{M2}}{\sigma_{SB} + 2 \cdot \sigma_{M2}} \cdot \overline{N}_{BF} = \alpha_2 \cdot \overline{N}_{BF} \tag{24}$$

It is immediate that $\alpha_1 + 2 \cdot \alpha_2 = 1$, $\alpha_1, \alpha_2 \geq 0$. In actual experiments, not always $\overline{N}$ events occur but the number of occurrences, N, is distributed around $\overline{N}$, such that $\overline{N} - \Delta\overline{N} \leq N \leq \overline{N} + \Delta\overline{N}$. In general, if $\overline{N} \gg 1$, the probability distribution for occurrences will be similar to a Poisson's distribution with $\Delta\overline{N} = q \cdot \sqrt{\overline{N}}$, q being a real number depending on the confidence and $\sqrt{N}$ the standard deviation in a Poisson's distribution.

Now, let us suppose that we have developed a procedure to extract MCUs from SBUs, able to detect all the 2-bit events but, unfortunately, it erroneously identifies false ones as well. As explained in Section II, the number of false pairs is proportional to $N_P \approx 0.5 \cdot N_{BF}^2$ so $\overline{N}_{FM2} \approx 0.5 \cdot L_X^{-1} \cdot N_{BF}^2 \cdot S_1$. For simplicity, in this approach, we have used N_{BF} instead of N_{SB}. The number of observed 2-bit MCUs will be:

$$O_{M2} = N_{M2} + N_{FM2} \implies N_{M2} = O_{M2} - N_{FM2} \tag{25}$$

As $\Delta\,(a - b) = \sqrt{(\Delta a)^2 + (\Delta b)^2}$, one can deduce that:

$$(\Delta N_{M2})^2 = (\Delta O_{M2})^2 + (\Delta N_{FM2})^2 =$$
$$= q^2 \cdot O_{M2} + q^2 \cdot N_{FM2} = q^2 \cdot \left(\alpha_2 \cdot N_{BF} + k \cdot N_{BF}^2\right)$$

with $k = 0.5 \cdot L_X^{-1} \cdot 0.5 \cdot S_1$. Combining this expression with (24) allows defining the relative error as the Figure Of Merit (F.O.M.):

$$F.O.M._{M2} = \frac{\Delta N_{M2}}{N_{M2}} = q \cdot \frac{\sqrt{1 + \frac{k}{\alpha_2} \cdot N_{BF}}}{\sqrt{\alpha_2} \cdot \sqrt{N_{BF}}} \tag{26}$$

As $O_{SB} = N_{SB} - 2 \cdot N_{FP} \implies N_{SB} = O_{SB} + 2 \cdot N_{FP}$, another F.O.M. can be determined:

$$F.O.M._{SB} = \frac{\Delta N_{SB}}{N_{SB}} = q \cdot \frac{\sqrt{1 + \frac{4k}{\alpha_1} \cdot N_{BF}}}{\sqrt{\alpha_1} \cdot \sqrt{N_{BF}}} \tag{27}$$

These expressions are infinite for $N_{BF} \to 0$ but they decrease with N_{BF}. Ideally, one would expect them to become zero to obtain a perfect measurement. However, neither of them finally reaches zero, but asymptotically tend to:

$$\lim_{N_{BF} \to \infty} F.O.M._{M2} = m \cdot \alpha_2^{-1} \cdot \sqrt{k} \tag{28}$$

$$\lim_{N_{BF} \to \infty} F.O.M._{SB} = m \cdot \alpha_1^{-1} \cdot \sqrt{4k} \tag{29}$$

However high N_{BF} may be, the relative error in the measurement will never be lower than the previous thresholds. Let us put an illustrating example. In [6], a 90-nm memory with $L_N = 2^{24}$ bits the SBU and 2-bit MCUs cross sections were respectively $\sigma_{SB} \sim 2.2 \cdot 10^{-15}$ cm^{-2} and $\sigma_{M2} \sim 3.3 \cdot 10^{-16}$ cm^{-2} at 3.3 V. Flipped cells were considered related to each other if the Manhattan Distance between them was 3 or lower. Therefore, $k = 7.15 \cdot 10^{-7}$ and $\alpha_1 = 0.76$, $\alpha_2 = 0.12$ so, using $q = 2$, which guarantees a confidence of around 95%. Eqs. 29 & 28 indicate that the numbers of SBUs and 2-bit MCUs cannot be known with an uncertainty lower than 0.4% and 2.9% using the data from a single experiment.

With identical data, a statistical test on the DV set was done to identify the MCUs and 12 anomalous values were identified. Therefore, k must be deduced from (9) taking into account that $L_A = 2^{21}$, yielding $k = 2.9 \cdot 10^{-6}$. In consequence, this method does not provide an uncertainty lower than 0.9 % for SBUs and 5.9 % for 2-bit MCUs.

This does not mean that the cross sections cannot be known with better accuracy since (28)-(29) are referred to a single experiment. However, if the experiment is repeated N_R times instead of just one, the error margin width of any parameter, with a random character, decreases with $N_R^{-1/2}$.

V. Conclusions

False multiple events can be erroneously identified at the time of analyzing data from radiation tests. However, the expected number of false 2-bit events can be accurately calculated independently of the method proposed to extract multiple events from the bulk of data using the concept of "cell influence area". Also, the number of false 3-bit events can be delimited. This family of identities has been backed up by both Monte Carlo simulations and actual experimental data. Some mathematical expressions can be used to process experimental data to get values closer to actual ones or, at least, to estimate the probability of erroneous detections with a family of birthday's statistics-like equations. Finally, it is demonstrated that it is not possible to get an arbitrary accuracy from a single round of radiation experiments.

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